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# IRFW630B

## N-Channel MOSFET

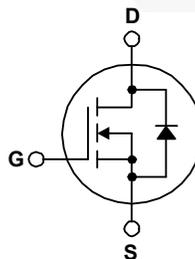
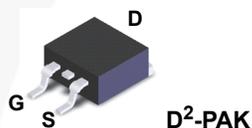
### 200 V, 9 A, 400 mΩ

#### Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters, switch mode power supplies, DC-AC converters for uninterrupted power supply and motor control.

#### Features

- 9.0 A, 200 V,  $R_{DS(on)} = 400 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 4.5 \text{ A}$
- Low Gate Charge (Typ. 22 nC)
- Low  $C_{rss}$  (Typ. 22 pF)
- 100% Avalanche Tested



#### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	IRFW630BTM_FP001	Unit
$V_{DSS}$	Drain-Source Voltage	200	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	9.0	A
	- Continuous ( $T_C = 100^\circ\text{C}$ )	5.7	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	36	A
$V_{GSS}$	Gate-Source voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	160	mJ
$I_{AR}$	Avalanche Current (Note 1)	9.0	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	7.2	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ )*	3.13	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	72	W
	- Derate above $25^\circ\text{C}$	0.57	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

#### Thermal Characteristics

Symbol	Parameter	IRFW630BTM_FP001	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.74	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Min. Pad of 2-oz Copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (*1 in <sup>2</sup> Pad of 2-oz Copper), Max.	40	

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
IRFW630B	IRFW630BTM_FP001	D <sup>2</sup> -PAK	330 mm	24 mm	800 units

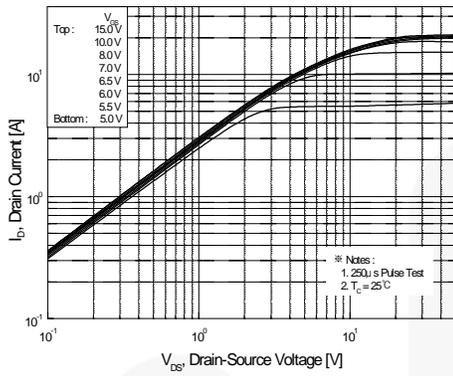
## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	200	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.2	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V	--	--	10	μA
		V <sub>DS</sub> = 160 V, T <sub>C</sub> = 125°C	--	--	100	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	--	4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.5 A	--	0.34	0.4	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 4.5 A	--	7.05	--	S
<b>Dynamic Characteristics</b>						
C <sub>iSS</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	550	720	pF
C <sub>oSS</sub>	Output Capacitance		--	85	110	pF
C <sub>rSS</sub>	Reverse Transfer Capacitance		--	22	29	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 100 V, I <sub>D</sub> = 9.0 A R <sub>G</sub> = 25 Ω	--	11	30	ns
t <sub>r</sub>	Turn-On Rise Time		--	70	150	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	60	130	ns
t <sub>f</sub>	Turn-Off Fall Time		(Note 4)	--	65	140
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 160 V, I <sub>D</sub> = 9.0 A V <sub>GS</sub> = 10 V	--	22	29	nC
Q <sub>gs</sub>	Gate-Source Charge		--	3.6	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		(Note 4)	--	10.2	--
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	9.0	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	36	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 9.0 A	--	--	1.5	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 9.0 A di <sub>F</sub> /dt = 100 A/μs	--	140	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	0.87	--	μC

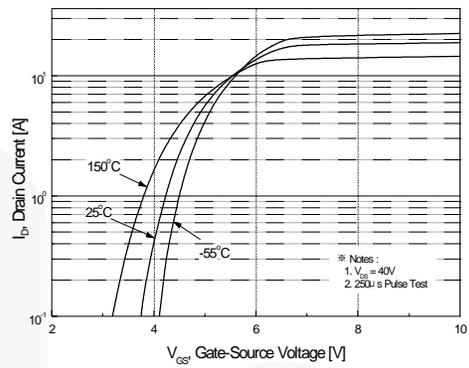
### Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L = 3 mH, I<sub>AS</sub> = 9.0 A, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25 Ω, starting T<sub>J</sub> = 25°C.
3. I<sub>SD</sub> ≤ 9.0 A, di/dt ≤ 300 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, starting T<sub>J</sub> = 25°C.
4. Essentially independent of operating temperature.

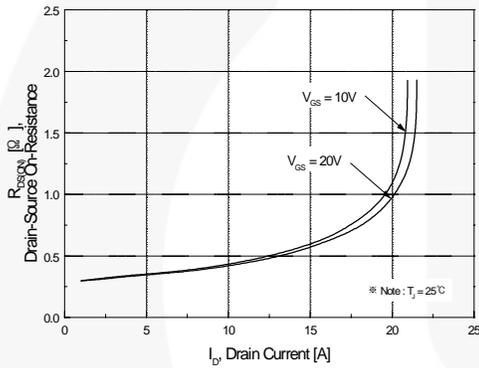
## Typical Characteristics



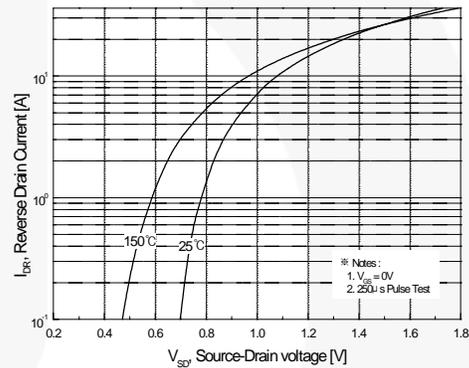
**Figure 1. On-Region Characteristics**



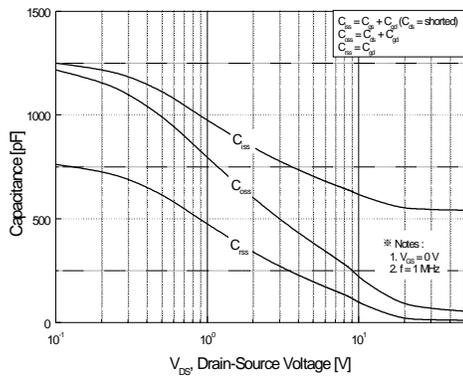
**Figure 2. Transfer Characteristics**



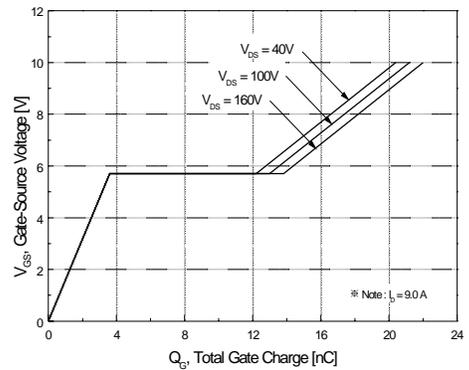
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



**Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature**



**Figure 5. Capacitance Characteristics**



**Figure 6. Gate Charge Characteristics**

Typical Characteristics (Continued)

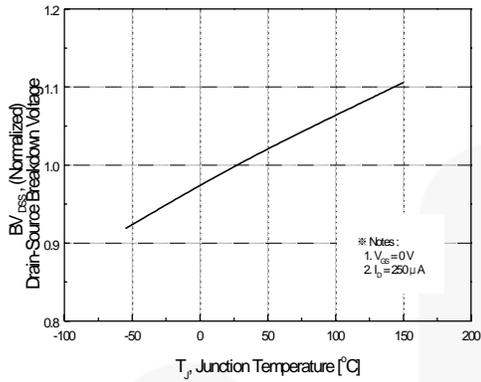


Figure 7. Breakdown Voltage Variation vs. Temperature

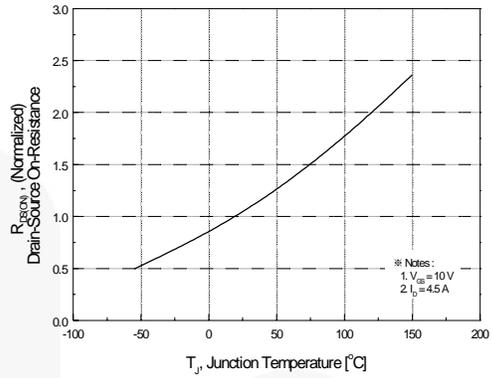


Figure 8. On-Resistance Variation vs. Temperature

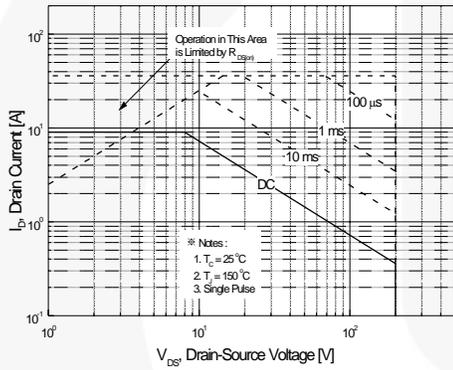


Figure 9. Maximum Safe Operating Area

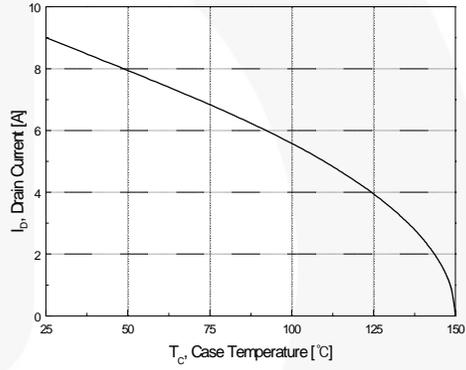


Figure 10. Maximum Drain Current vs. Case Temperature

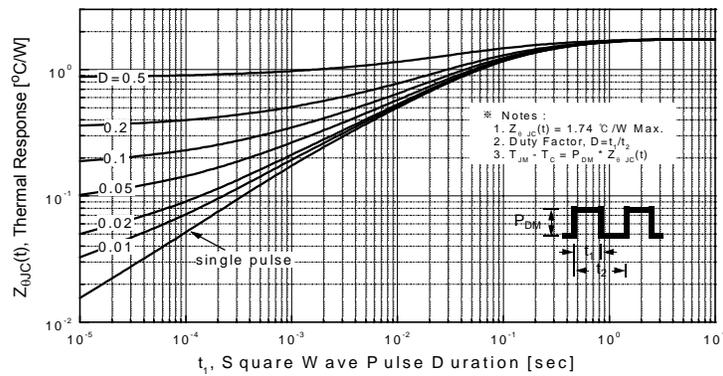


Figure 11. Transient Thermal Response Curve

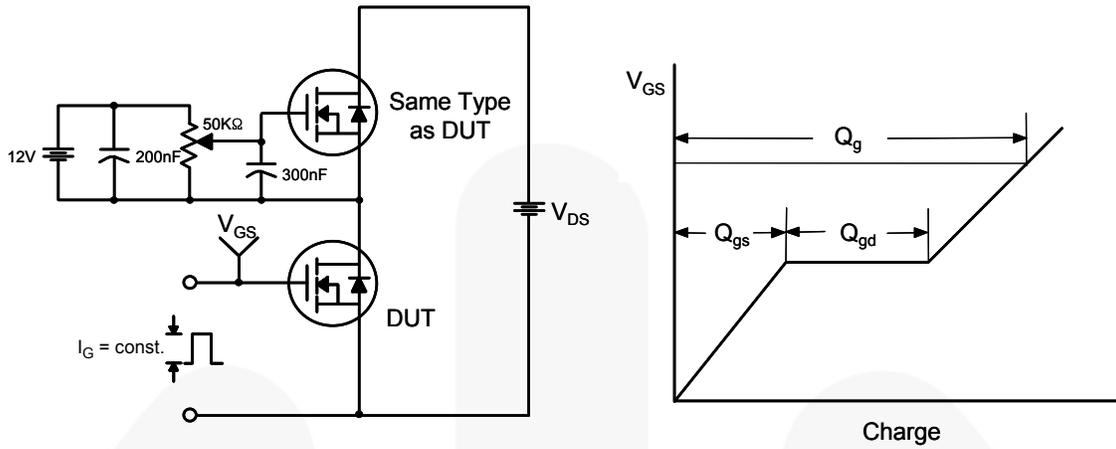


Figure 12. Gate Charge Test Circuit & Waveform

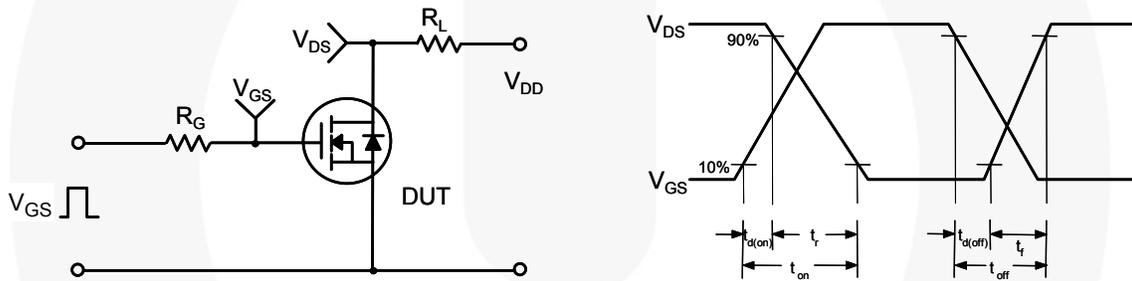


Figure 13. Resistive Switching Test Circuit & Waveforms

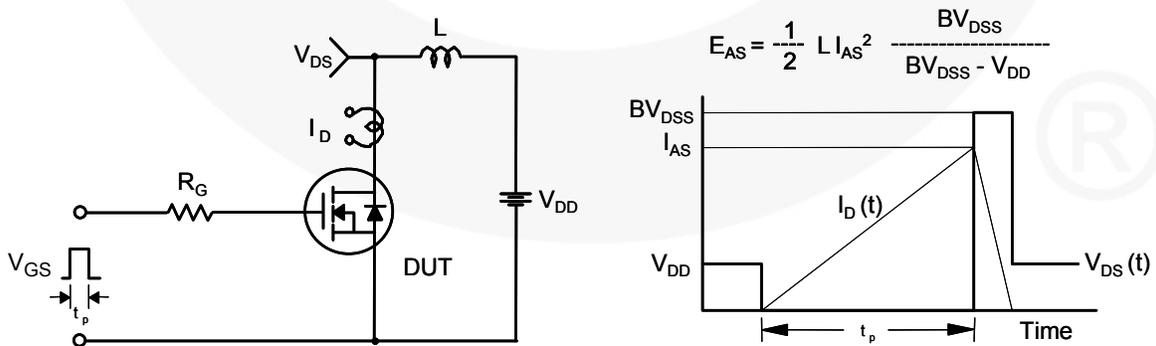


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

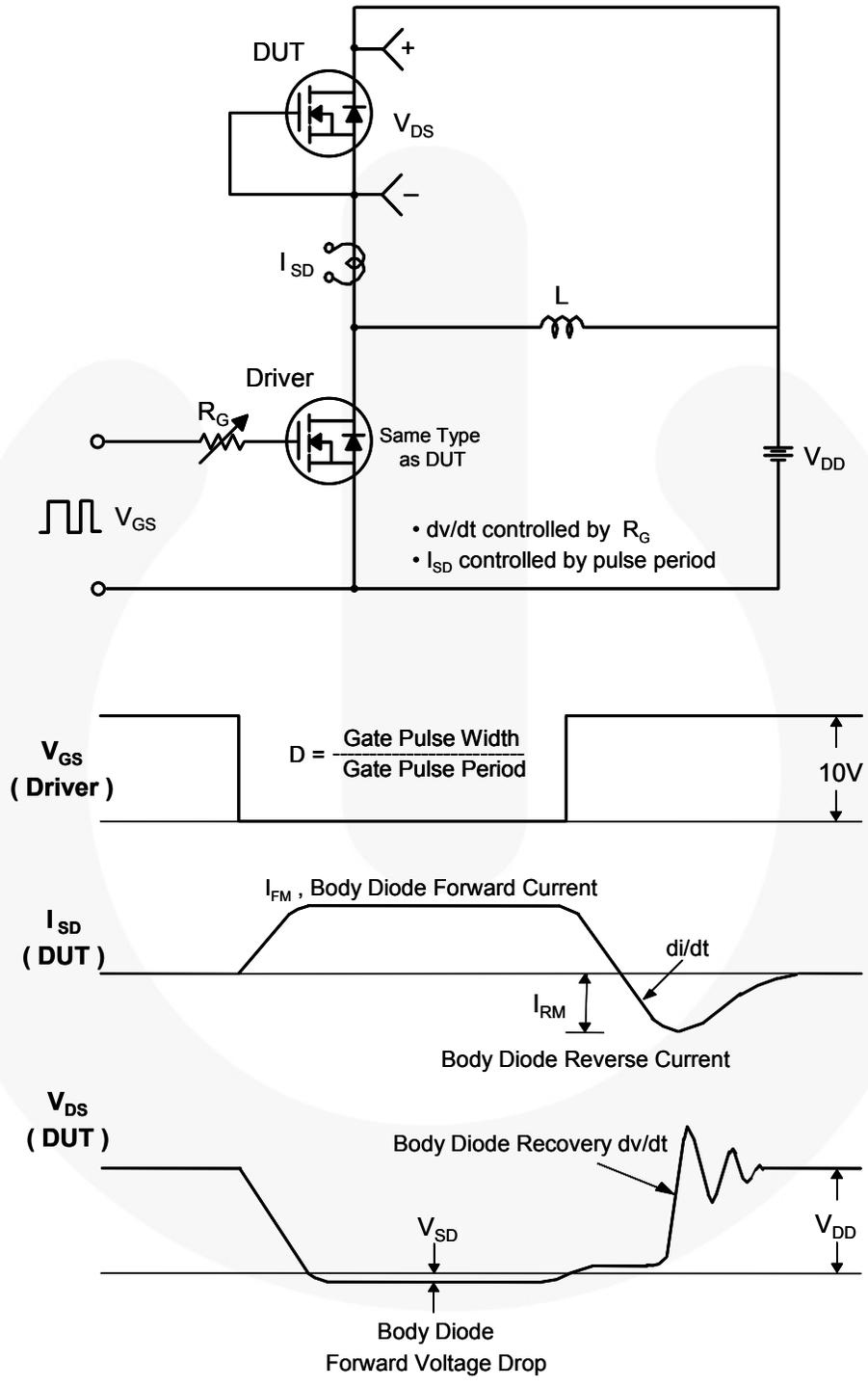


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms





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