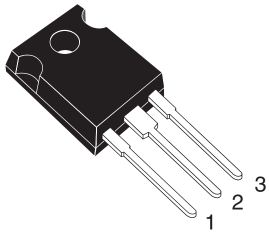
STW25N95K3

N-channel 950 V, 0.32 Ω, 22 A, TO-247 SuperMESH3™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D	Pw
STW25N95K3	950 V	< 0.36 Ω	22 A	400 W

- 100% avalanche tested
- Extremely large avalanche performance
- Gate charge minimized
- Very low intrinsic capacitances
- Zener-protected



TO-247

Application

- Switching applications

Description

This SuperMESH3™ Power MOSFET is the result of improvements applied to STMicroelectronics' SuperMESH™ technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

Figure 1. Internal schematic diagram

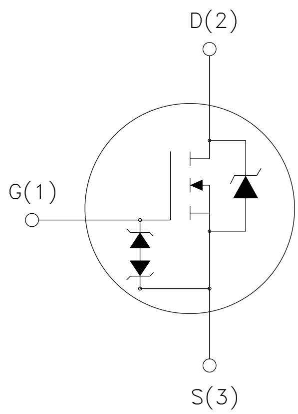


Table 1. Device summary

Order code	Marking	Package	Packaging
STW25N95K3	25N95K3	TO-247	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	22	A
I_D	Drain current (continuous) at T_C = 100 °C	13.9	A
I_{DM} (1)	Drain current (pulsed)	88	A
P_{TOT}	Total dissipation at T_C = 25 °C	400	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	28	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	450	mJ
dv/dt(2)	Peak diode recovery voltage slope	5	V/ns
$V_{ESD(G-S)}$	G-S ESD (HBM C=100 pF; R=1.5 kΩ)	6000	V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq$ 22 A, di/dt $\leq$ 100 A/µs, peak $V_{DS} \leq V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.31	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	50	°C/W
T_J	Maximum lead temperature for soldering purpose	300	°C/W

2 Electrical characteristics

(T_{case} =25°C unless otherwise specified).

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	950			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C			1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 150 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 11 A		0.32	0.36	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D = 11 A	-	22	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	3680 246 2	-	pF pF pF
$C_{o(tr)}$ (2)	Equivalent capacitance time related	V_{DS} = 0 to 760 V, V_{GS} = 0	-	198	-	pF
$C_{o(er)}$ (3)	Equivalent capacitance energy related	V_{DS} = 0 to 760 V, V_{GS} = 0	-	278	-	pF
R_g	Gate input resistance	f=1 MHz open drain	-	3	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 760 V, I_D = 22 A, V_{GS} = 10 V *(see Figure 16)*	-	105 23 57	-	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
3. $C_{oss\ eq.}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 475 V, I_D = 11 A, R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 15)*	-	39 29 97 59	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		22 88	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 22 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 22 A, di/dt = 100 A/µs V_{DD}= 60 V, T_J = 25 °C *(see Figure 17)*	-	671 17 50		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 22 A, di/dt = 100 A/µs V_{DD}= 60 V T_J = 150 °C *(see Figure 17)*	-	803 21 52		ns µC A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs=± 1 mA (open drain)	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

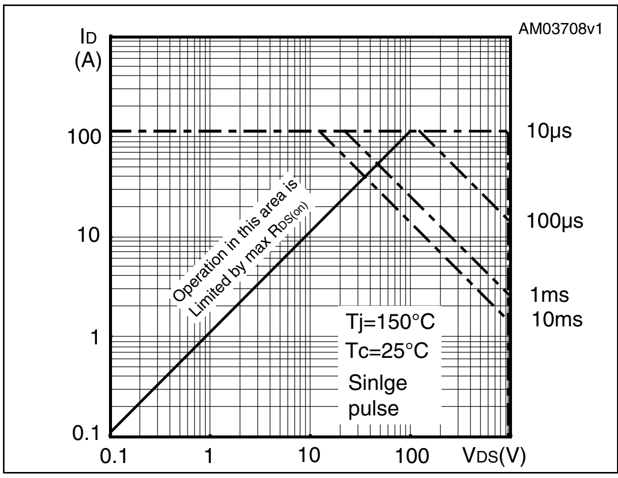


Figure 3. Thermal impedance

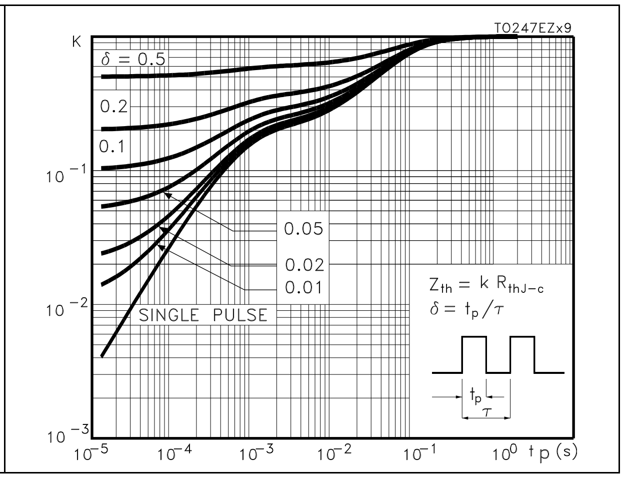


Figure 4. Output characteristics

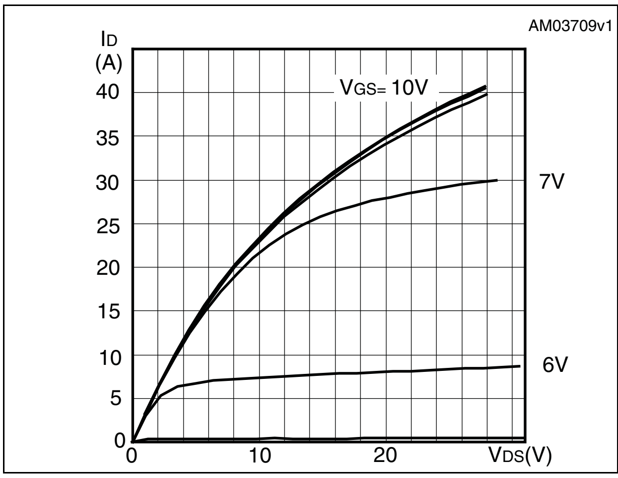


Figure 5. Transfer characteristics

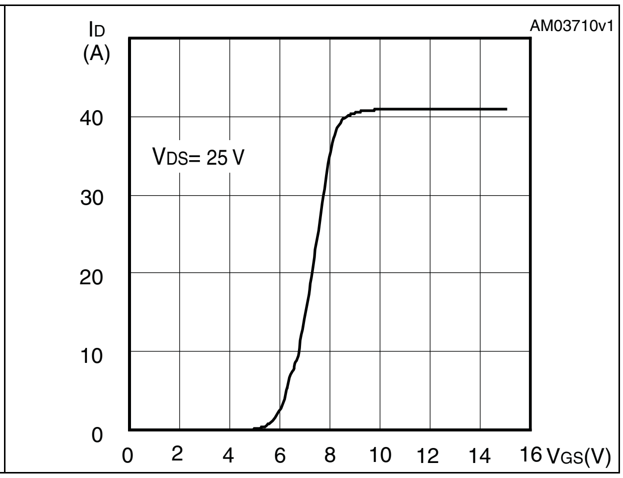


Figure 6. Normalized BV_{DSS} vs temperature

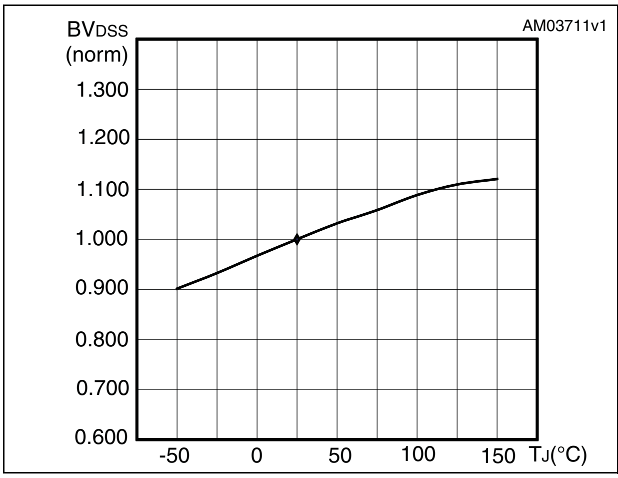


Figure 7. Static drain-source on resistance

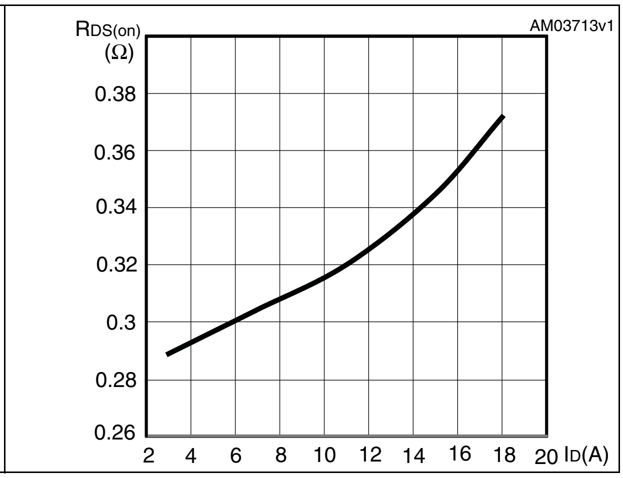


Figure 8. Output capacitance stored energy

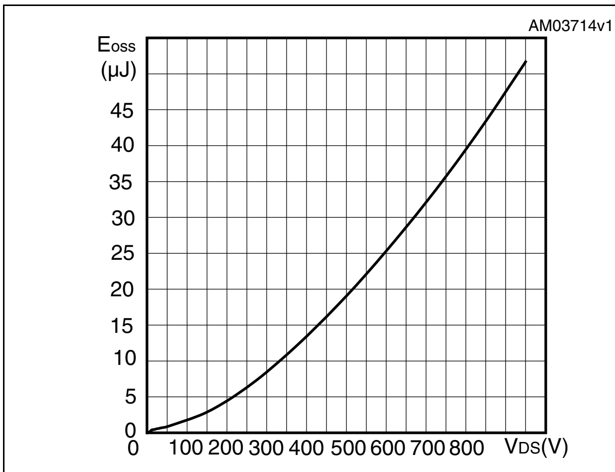


Figure 9. Capacitance variations

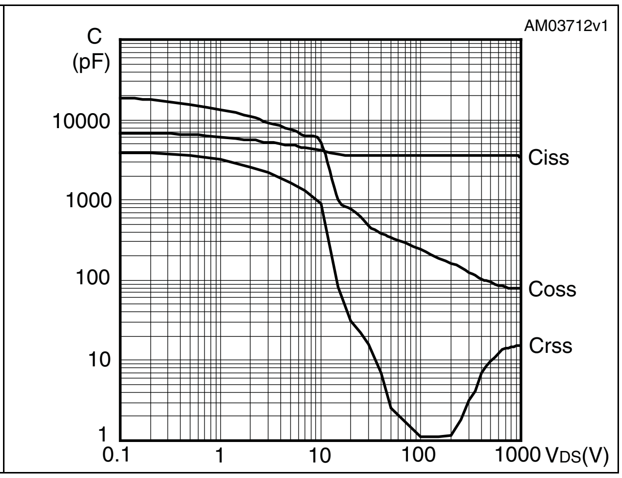


Figure 10. Gate charge vs gate-source voltage

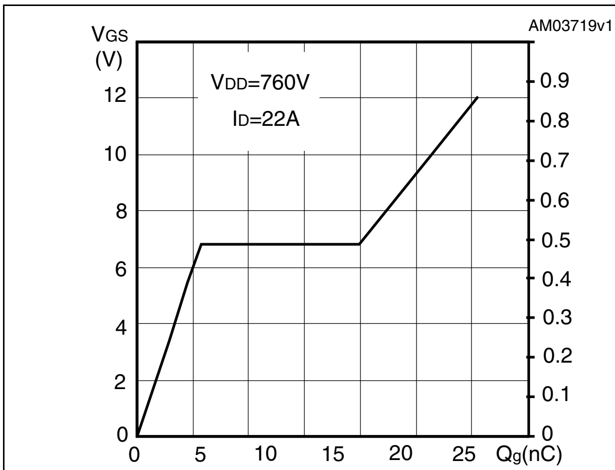


Figure 11. Normalized on resistance vs temperature

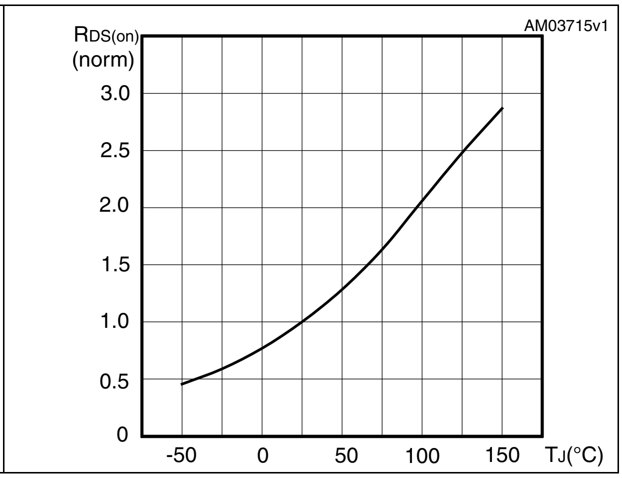


Figure 12. Normalized gate threshold voltage vs temperature

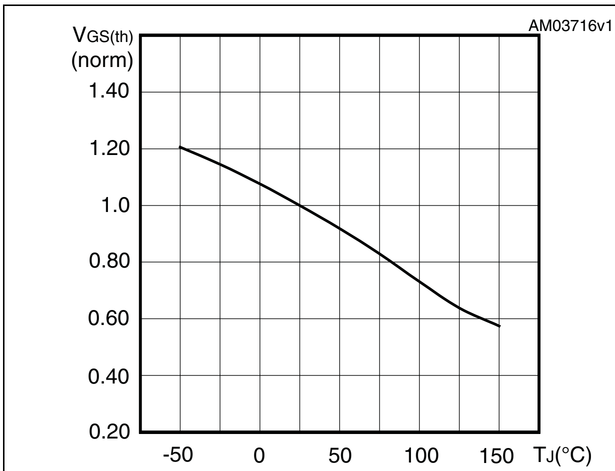


Figure 13. Maximum avalanche energy vs temperature

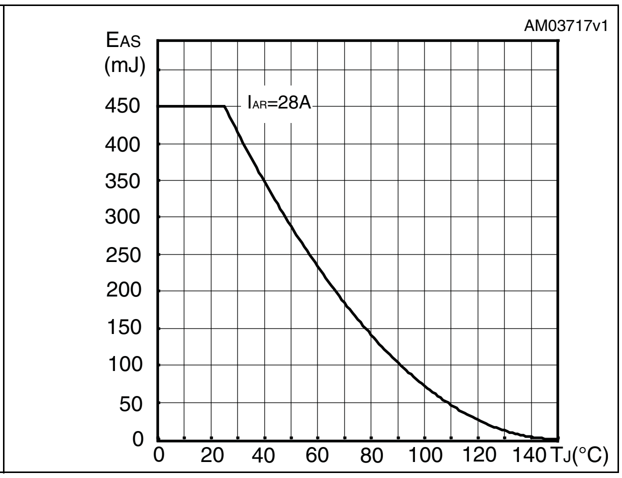
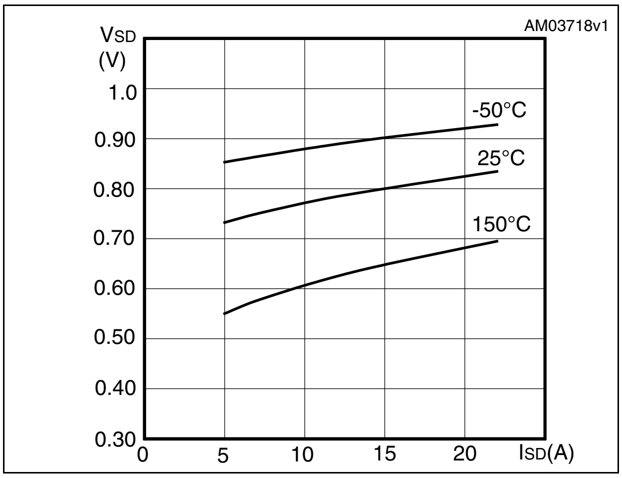


Figure 14. Source-drain diode forward characteristics



3 Test circuits

Figure 15. Switching times test circuit for resistive load

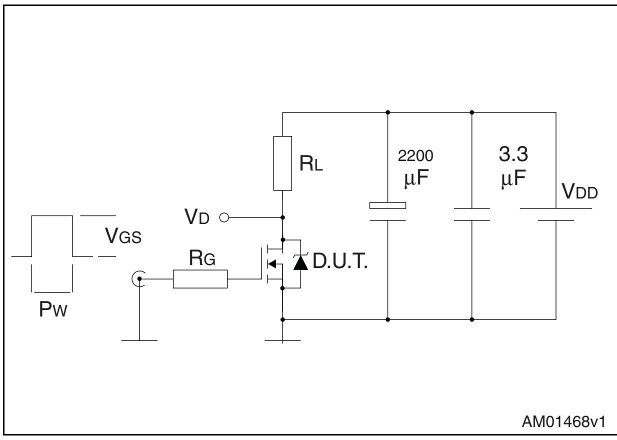


Figure 16. Gate charge test circuit

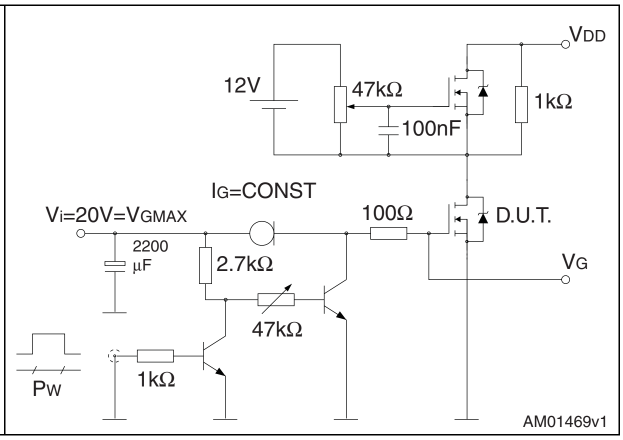


Figure 17. Test circuit for inductive load switching and diode recovery times

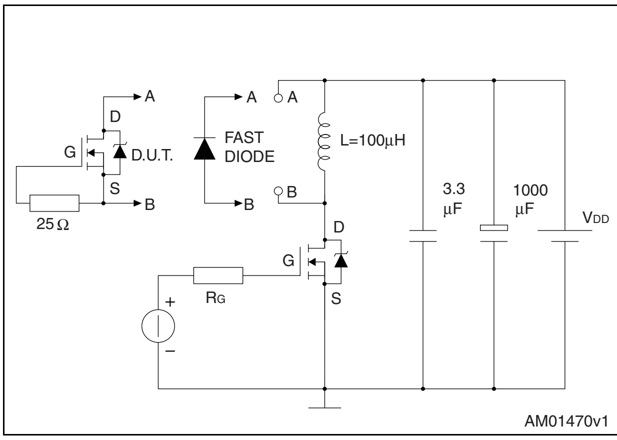


Figure 18. Unclamped inductive load test circuit

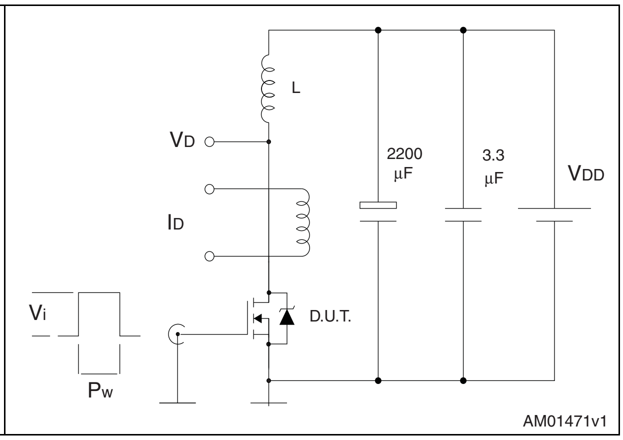


Figure 19. Unclamped inductive waveform

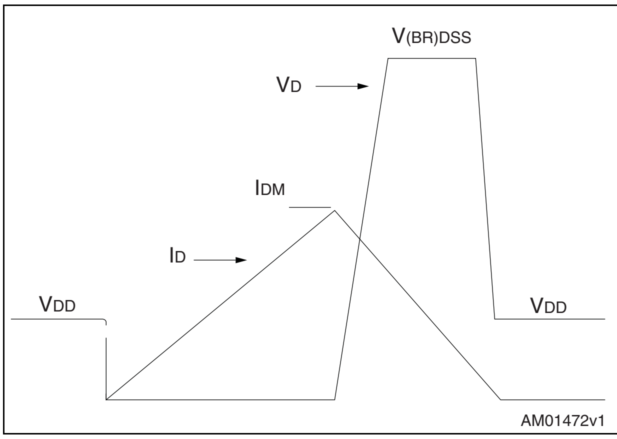
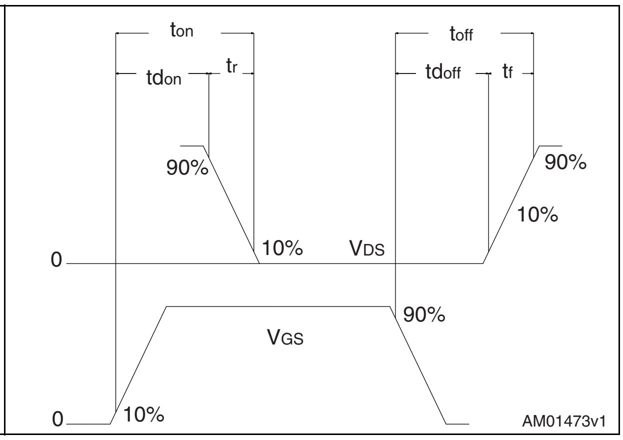


Figure 20. Switching time waveform



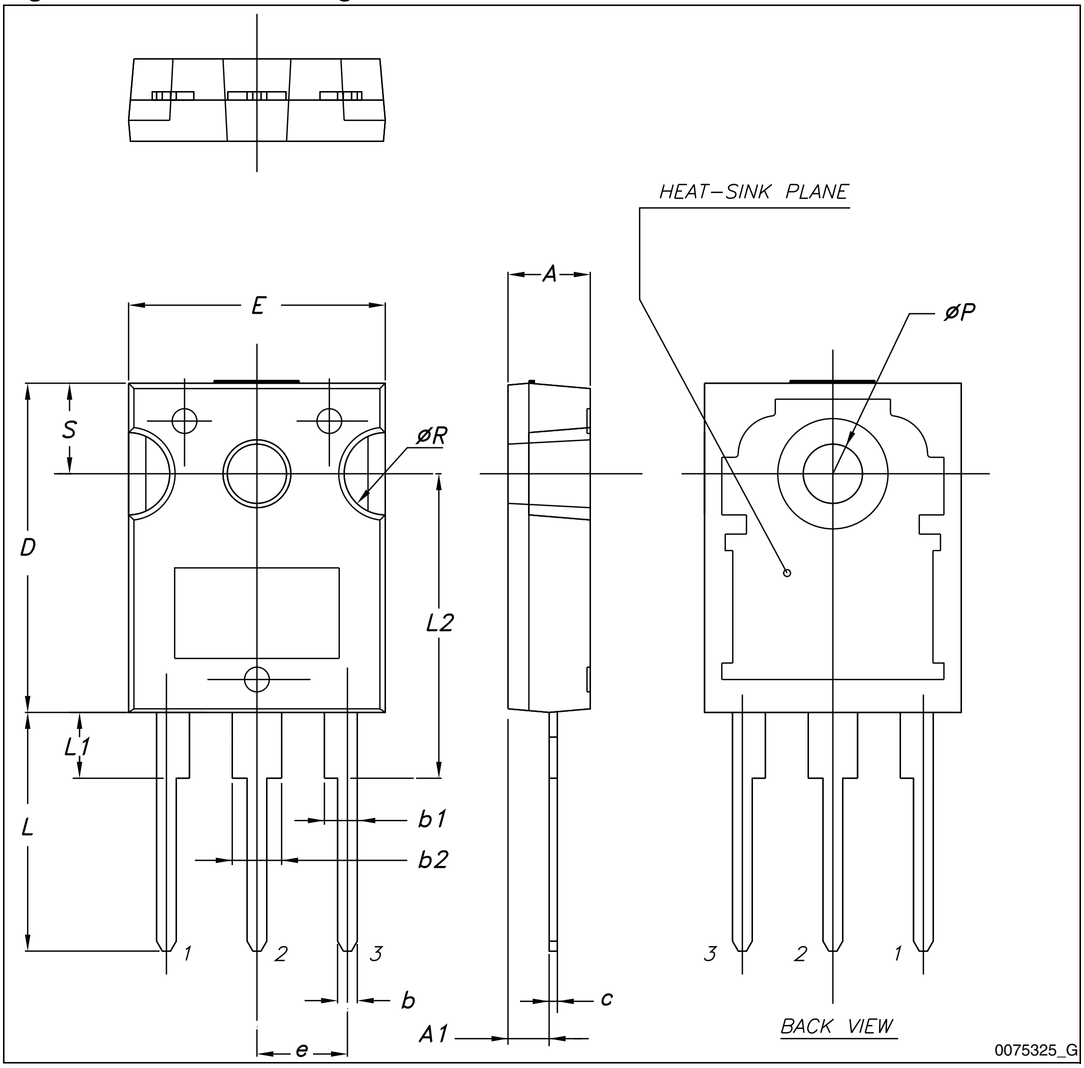
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
∅P	3.55		3.65
∅R	4.50		5.50
S	5.30	5.50	5.70

Figure 21. TO-247 drawing



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
27-Apr-2009	1	First release.
09-Jan-2012	2	Document status promoted from preliminary data to datasheet. Updated *Section 4: Package mechanical data*.