

BUK963R1-40E

N-channel TrenchMOS logic level FET

13 July 2012

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with Vgst(th) rating of greater than 0.5V at 175 °C

1.3 Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	40	V
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; <u>Fig. 1</u>	[1]	-	-	100	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>		-	-	234	W
Static characte	eristics						,
R _{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C}; Fig. 11$		-	2.6	3.1	mΩ
Dynamic chara	acteristics						
Q_{GD}	gate-drain charge	V _{GS} = 5 V; I _D = 25 A; V _{DS} = 32 V; Fig. 13; Fig. 14		-	25.8	-	nC

[1] Continuous current is limited by package.



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	mb	D
2	D	drain		
3	S	source		G_U: 4
mb	D	mounting base; connected to drain	D2PAK (SOT404)	mbb076 S

3. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
BUK963R1-40E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404		

4. Limiting values

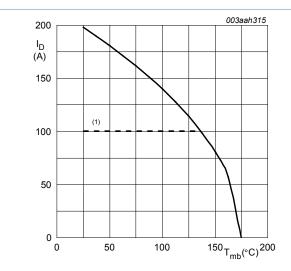
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \ge 25 ^{\circ}\text{C}; T_j \le 175 ^{\circ}\text{C}$		-	40	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 k Ω		-	40	V
V_{GS}	gate-source voltage	T _j = 25 °C		-10	10	V
		T_j = 25 °C; lifetime = 100 hours		-15	15	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 5 V; <u>Fig. 1</u>	[1]	-	100	Α
		T _{mb} = 100 °C; V _{GS} = 5 V; <u>Fig. 1</u>	[1]	-	100	Α
I _{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \mu s$; Fig. 4		-	794	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>		-	234	W
T _{stg}	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
Source-dra	ain diode					
Is	source current	T _{mb} = 25 °C	[1]	-	100	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	794	Α

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche rug	ggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 100 A; $V_{sup} \le$ 40 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 3	[2][3]	-	419	mJ

- [1]
- Continuous current is limited by package. Single-pulse avalanche rating limited by maximum junction temperature of 175 $^{\circ}\text{C}.$
- Refer to application note AN10273 for further information.



(1) Capped at 100A due to package

Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \ge 5V$$

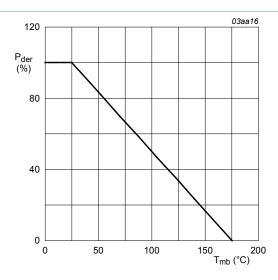
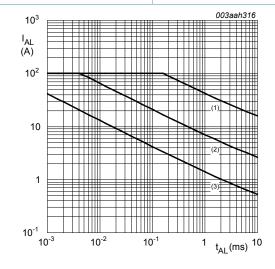


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$



Single pulse avalanche rating; avalanche current as a function of avalanche time

(1)
$$T_{j \text{ (init)}} = 25^{\circ}C$$
; (2) $T_{j \text{ (init)}} = 150^{\circ}C$; (3) Repetitive Avalanche

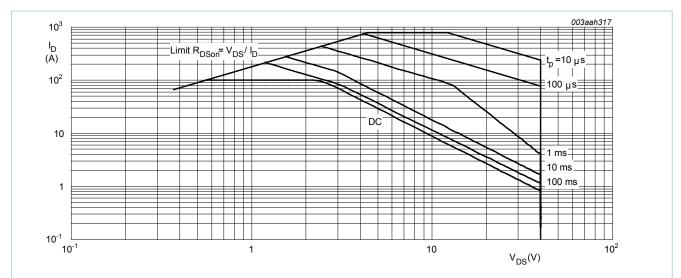


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

 $T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 5	-	-	0.64	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board	-	50	-	K/W

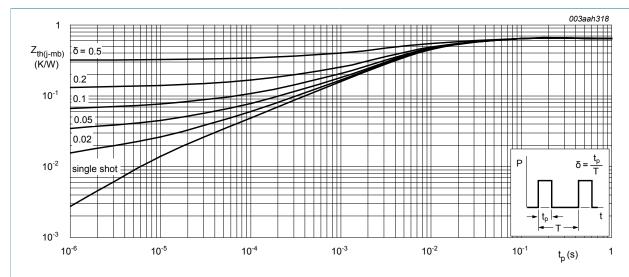


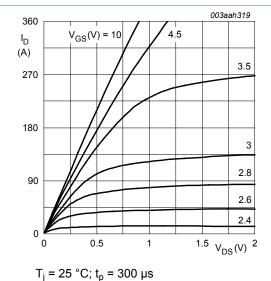
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	aracteristics		'			
V _{(BR)DSS}	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 ^{\circ}C$	40	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	36	-	-	V
(-)	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 25 °C; Fig. 9; Fig. 10	1.4	1.7	2.1	V
		I_D = 1 mA; V_{DS} = V_{GS} ; T_j = -55 °C; Fig. 9	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C};$ Fig. 9	0.5	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _j = 25 °C	-	0.06	1	μA
		V _{DS} = 40 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state	V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; <u>Fig. 11</u>	-	2.6	3.1	mΩ
	resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 11	-	2.25	2.7	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 175 °C; Fig. 12; Fig. 11	-	-	6	mΩ
Dynamic	characteristics					
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 32 V; V _{GS} = 5 V;	-	69.5	-	nC
Q_{GS}	gate-source charge	Fig. 13; Fig. 14	-	16.1	-	nC
Q_{GD}	gate-drain charge		-	25.8	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz;	-	6870	9150	pF
C _{oss}	output capacitance	T _j = 25 °C; <u>Fig. 15</u>	-	875	1050	pF
C _{rss}	reverse transfer capacitance		-	450	620	pF
t _{d(on)}	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω ; V_{GS} = 5 V;	-	42	-	ns
t _r	rise time	$R_{G(ext)} = 5 \Omega$	-	73	-	ns
t _{d(off)}	turn-off delay time		-	114	-	ns
t _f	fall time		-	76	-	ns
L _D	internal drain inductance	from upper edge of drain mounting base to center of die	-	2.5	-	nH
L _S	internal source inductance	from source lead to source bonding pad	-	7.5	-	nΗ

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 16$		-	0.8	1.2	V
t _{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$		-	40	-	ns
Q _r	recovered charge	V _{DS} = 25 V		-	47	-	nC



Output characteristics; drain current as a

function of drain-source voltage; typical values

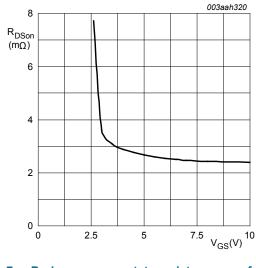


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25^{\circ}C; I_D = 25A$$

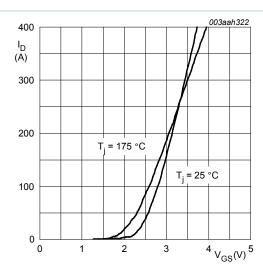


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

 $V_{DS} = 10V$

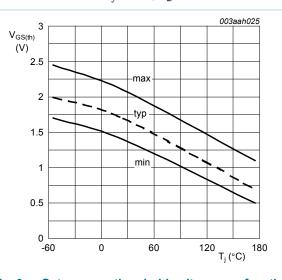


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; \ V_{DS} = V_{GS}$$

Fig. 6.

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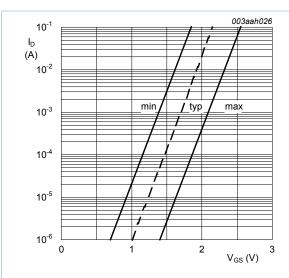


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^{\circ}C; \ V_{DS} = 5V$$

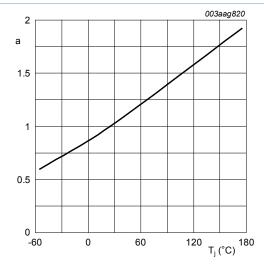
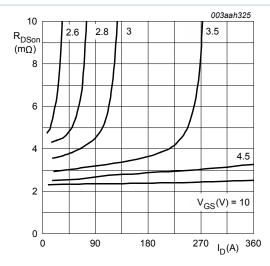


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$\mathbf{a} = \frac{R_{DSon}}{R_{DSon(25 \, \text{C})}}$$



$$T_j = 25 \, ^{\circ}C; t_p = 300 \, \mu s$$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

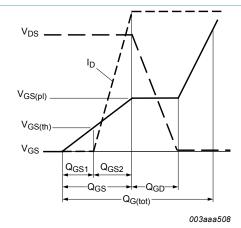


Fig. 13. Gate charge waveform definitions

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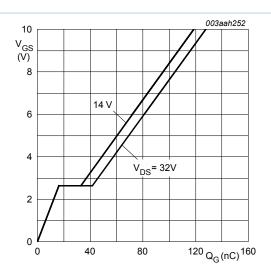


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^{\circ}C; I_D = 25A$$

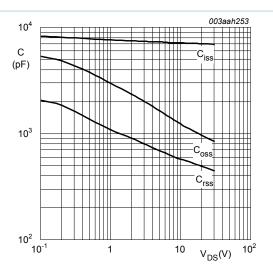


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = \mathbf{0}V$$
; $f = \mathbf{1}MHz$

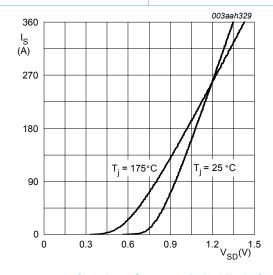


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

7. Package outline

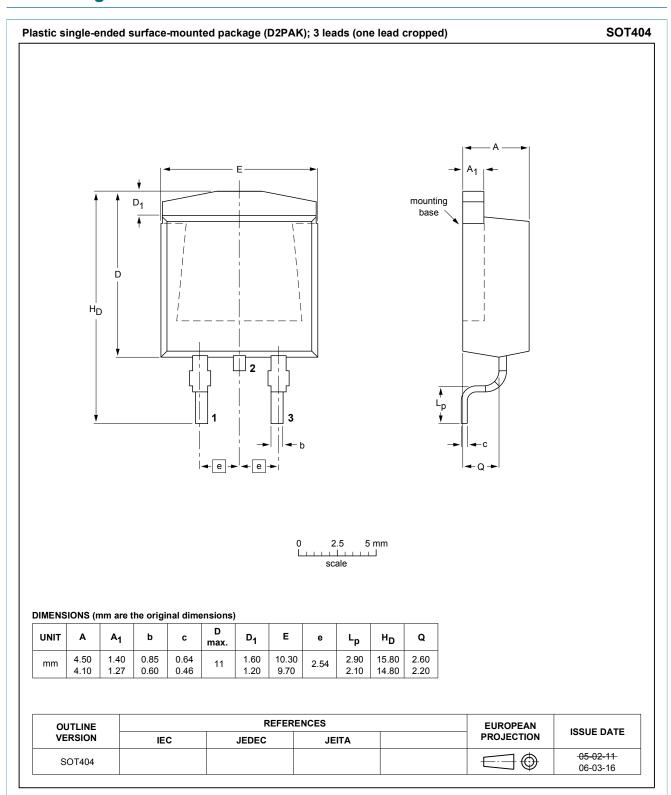


Fig. 17. D2PAK (SOT404)

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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