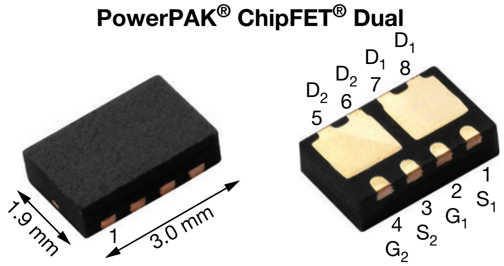
# Dual N-Channel 30 V (D-S) MOSFET

**PowerPAK® ChipFET® Dual**




Top View    Bottom View

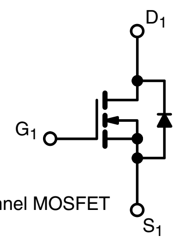
## FEATURES

- TrenchFET® power MOSFET
- 100 % $R_g$ and UIS tested
- New thermally enhanced PowerPAK® ChipFET® package
  - Small footprint area
  - Low on-resistance
  - Thin 0.8 mm profile
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

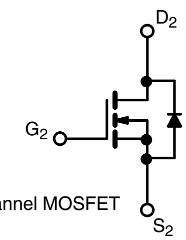
Pb-free
RoHS COMPLIANT
HALOGEN FREE

## APPLICATIONS

- DC/DC power supply




N-Channel MOSFET




N-Channel MOSFET

| PRODUCT SUMMARY | | | |
|---|---|---|---|
| $V_{DS}$ (V) | $R_{DS(on)}$ (Ω) MAX. | $I_D$ (A) | $Q_g$ (TYP.) |
| 30 | 0.0192 at $V_{GS}$ = 10 V | 6 [a] | 4.7 nC |
| | 0.0220 at $V_{GS}$ = 6 V | 6 [a] | |
| | 0.0245 at $V_{GS}$ = 4.5 V | 6 [a] | |

**Marking Code:** CG

**Ordering Information:**
Si5922DU-T1-GE3 (lead (Pb)-free and halogen-free)

| ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C, unless otherwise noted) | | | | |
|---|---|---|---|---|
| PARAMETER | | SYMBOL | LIMIT | UNIT |
| Drain-Source Voltage | | $V_{DS}$ | 30 | V |
| Gate-Source Voltage | | $V_{GS}$ | +20 / -16 | |
| Continuous Drain Current ($T_J$ = 150 °C) | $T_C$ = 25 °C | $I_D$ | 6 [a] | A |
| | $T_C$ = 70 °C | | 6 [a] | |
| | $T_A$ = 25 °C | | 6 [a, b, c] | |
| | $T_A$ = 70 °C | | 6 [a, b, c] | |
| Pulsed Drain Current (t = 100 μs) | | $I_{DM}$ | 24 | |
| Continuous Source-Drain Diode Current | $T_C$ = 25 °C | $I_S$ | 6 [a] | |
| | $T_A$ = 25 °C | | 1.9 [b, c] | |
| Single Pulse Avalanche Current | L = 0.1 mH | $I_{AS}$ | 10 | |
| Avalanche Energy | | $E_{AS}$ | 5 | mJ |
| Maximum Power Dissipation | $T_C$ = 25 °C | $P_D$ | 10.4 | W |
| | $T_C$ = 70 °C | | 6.7 | |
| | $T_A$ = 25 °C | | 2.3 [b, c] | |
| | $T_A$ = 70 °C | | 1.5 [b, c] | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | -55 to +150 | °C |
| Soldering Recommendations (Peak Temperature) [d, e] | | | 260 | |

| THERMAL RESISTANCE RATINGS | | | | | |
|---|---|---|---|---|---|
| PARAMETER | | SYMBOL | TYPICAL | MAXIMUM | UNIT |
| Maximum Junction-to-Ambient [b, f] | t ≤ 5 s | $R_{thJA}$ | 43 | 55 | °C/W |
| Maximum Junction-to-Case (Drain) | Steady State | $R_{thJC}$ | 9.5 | 12 | |

**Notes**

a. Package limited.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 5 s.
d. See solder profile (www.vishay.com/ppg?73257). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state conditions is 105 °C/W.

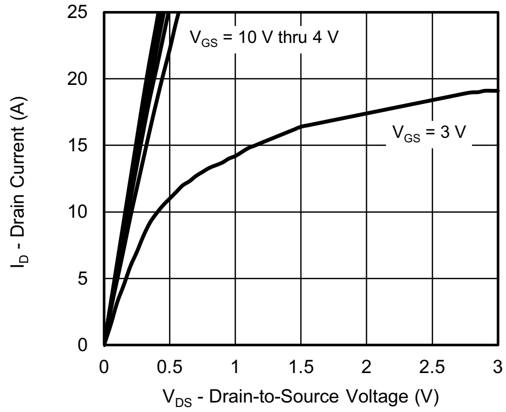
| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 30 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | $I_D$ = 250 μA | - | 14.3 | - | mV/°C |
| $V_{GS(th)}$ Temperature Coefficient | $\Delta V_{GS(th)}/T_J$ | | - | -4.7 | - | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 1.2 | - | 2.2 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = +20 V / -16 V | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 30 V, $V_{GS}$ = 0 V | - | - | 1 | μA |
| | | $V_{DS}$ = 30 V, $V_{GS}$ = 0 V, $T_J$ = 55 °C | - | - | 10 | |
| On-State Drain Current [a] | $I_{D(on)}$ | $V_{DS} \geq$ 5 V, $V_{GS}$ = 10 V | 5 | - | - | A |
| Drain-Source On-State Resistance [a] | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 5 A | - | 0.0155 | 0.0192 | Ω |
| | | $V_{GS}$ = 6 V, $I_D$ = 4 A | - | 0.0170 | 0.0220 | |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 4 A | - | 0.0190 | 0.0245 | |
| Forward Transconductance [a] | $g_{fs}$ | $V_{DS}$ = 10 V, $I_D$ = 5 A | - | 22 | - | S |
| **Dynamic** [b] | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1 MHz | - | 765 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 225 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 14 | - | |
| $C_{rss}/C_{iss}$ Ratio | | | - | 0.018 | 0.036 | - |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 15 V, $V_{GS}$ = 10 V, $I_D$ = 5 A | - | 10 | 15 | nC |
| | | $V_{DS}$ = 15 V, $V_{GS}$ = 4.5 V, $I_D$ = 5 A | - | 4.7 | 7.1 | |
| Gate-Source Charge | $Q_{gs}$ | | - | 2.2 | - | |
| Gate-Drain Charge | $Q_{gd}$ | | - | 0.65 | - | |
| Output Charge | $Q_{oss}$ | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V | - | 6.5 | - | |
| Gate Resistance | $R_g$ | f = 1 MHz | 1.3 | 6.3 | 12.6 | Ω |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 15 V, $R_L$ = 3 Ω<br>$I_D \cong$ 5 A, $V_{GEN}$ = 10 V, $R_g$ = 1 Ω | - | 6 | 15 | ns |
| Rise Time | $t_r$ | | - | 25 | 50 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 15 | 30 | |
| Fall Time | $t_f$ | | - | 10 | 20 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 15 V, $R_L$ = 3 Ω<br>$I_D \cong$ 5 A, $V_{GEN}$ = 4.5 V, $R_g$ = 1 Ω | - | 17 | 35 | |
| Rise Time | $t_r$ | | - | 45 | 90 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 16 | 30 | |
| Fall Time | $t_f$ | | - | 27 | 50 | |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | $T_C$ = 25 °C | - | - | 6 | A |
| Pulse Diode Forward Current (t = 100 μs) | $I_{SM}$ | | - | - | 24 | |
| Body Diode Voltage | $V_{SD}$ | $I_S$ = 5 A, $V_{GS}$ = 0 V | - | 0.81 | 1.2 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $I_F$ = 5 A, dI/dt = 100 A/μs, $T_J$ = 25 °C | - | 21 | 40 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | - | 10 | 20 | nC |
| Reverse Recovery Fall Time | $t_a$ | | - | 12 | - | ns |
| Reverse Recovery Rise Time | $t_b$ | | - | 9 | - | |

**Notes**

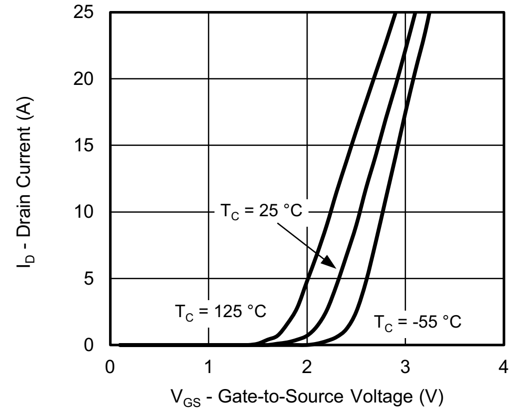
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

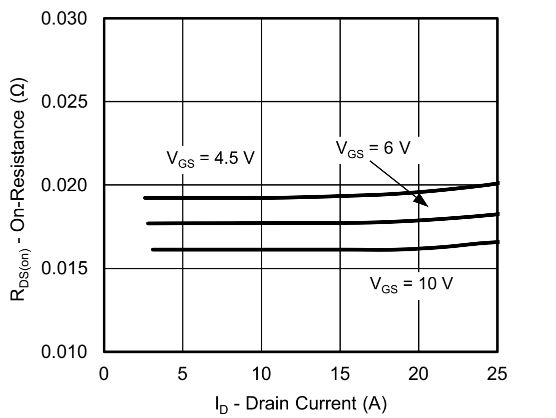
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



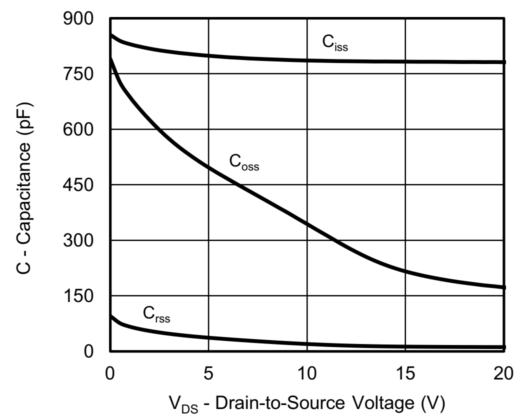

**Output Characteristics**



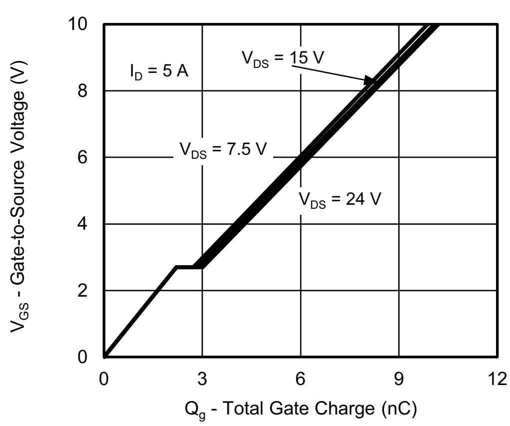

**Transfer Characteristics**



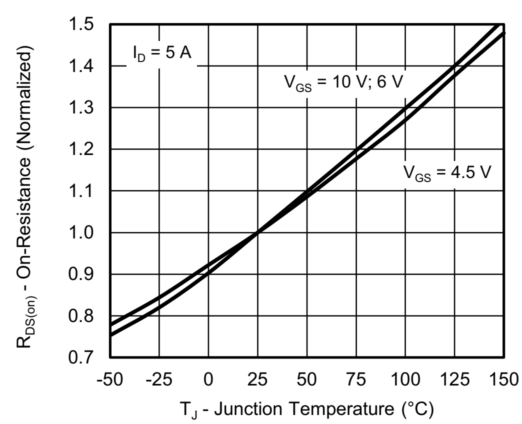

**On-Resistance vs. Drain Current and Gate Voltage**




**Capacitance**

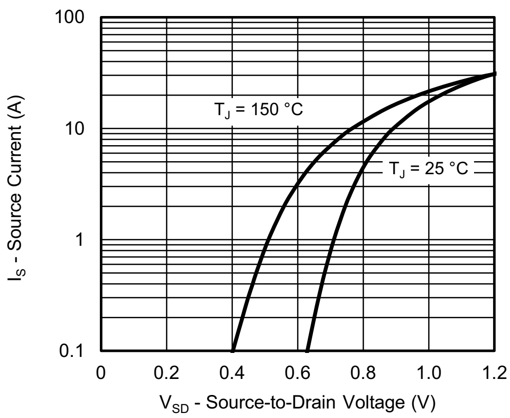



**Gate Charge**

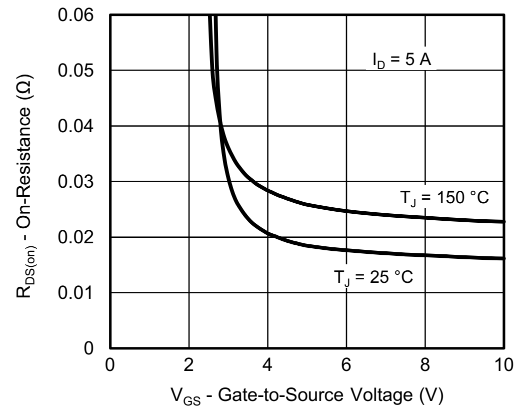



**On-Resistance vs. Junction Temperature**

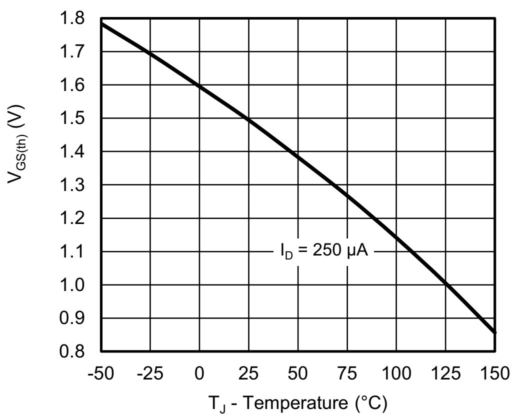
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



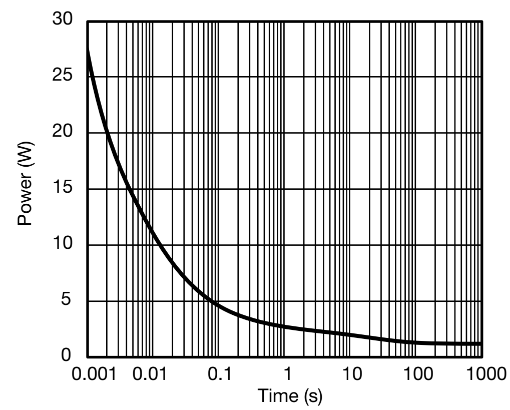

**Source-Drain Diode Forward Voltage**



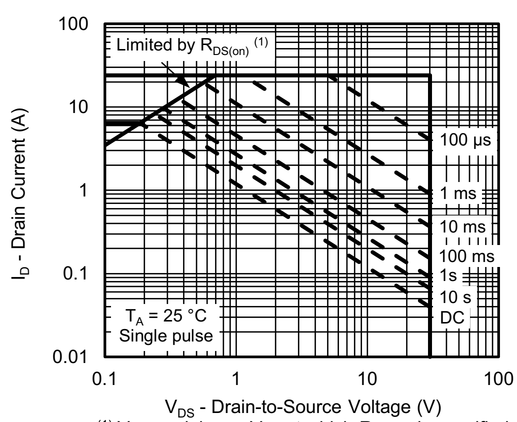

**On-Resistance vs. Gate-to-Source Voltage**




**Threshold Voltage**



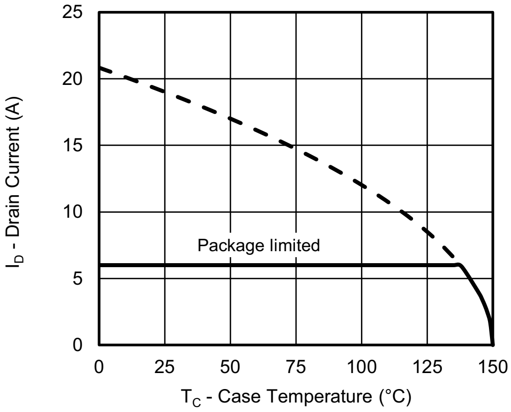

**Single Pulse Power, Junction-to-Ambient**



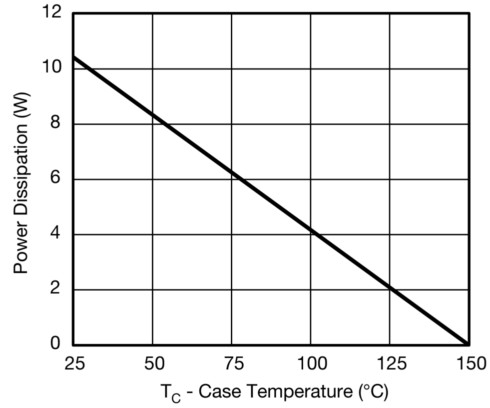

(1) $V_{GS}$ > minimum $V_{GS}$ at which $R_{DS(on)}$ is specified

**Safe Operating Area**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)




**Current Derating** [a]

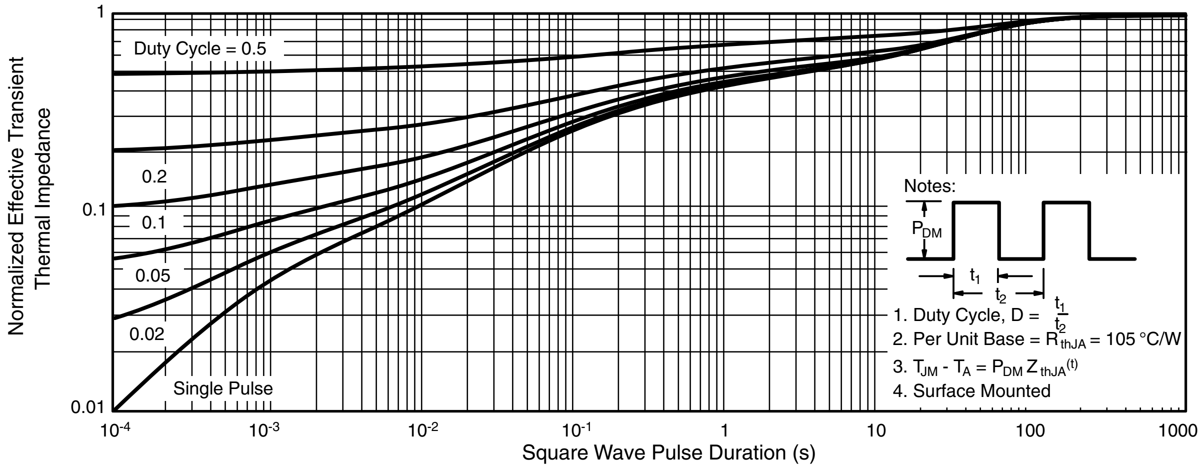



**Power Derating**

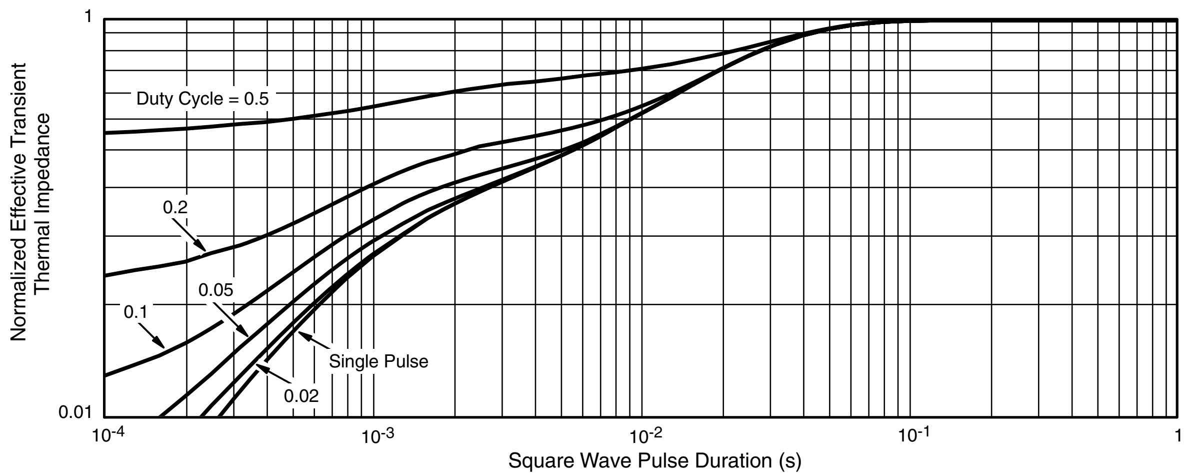
**Note**

a. The power dissipation $P_D$ is based on $T_J$ (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)




**Normalized Thermal Transient Impedance, Junction-to-Ambient**




**Normalized Thermal Transient Impedance, Junction-to-Case**

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