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Kind regards,

Team Nexperia



# PHK31NQ03LT

N-channel TrenchMOS logic level FET

Rev. 3 — 11 March 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

### 1.3 Applications

- DC-to-DC converters
- Notebook computers
- Switched-mode power supplies
- Voltage regulators

### 1.4 Quick reference data

Table 1. Quick reference data

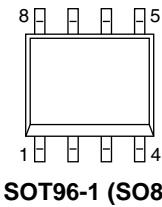
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25^\circ\text{C}; T_j \leq 150^\circ\text{C}$	-	-	30	V
$I_D$	drain current	$T_{sp} = 25^\circ\text{C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	-	30.4	A
$P_{tot}$	total power dissipation	$T_{sp} = 25^\circ\text{C}$ ; see <a href="#">Figure 2</a>	-	-	6.9	W
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ $T_j = 25^\circ\text{C}$ ; see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	-	3.45	4.4	$\text{m}\Omega$
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 4.5\text{ V}; I_D = 25\text{ A};$ $V_{DS} = 12\text{ V}$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	7.7	-	nC



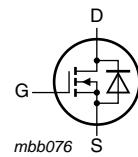
## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		



SOT96-1 (SO8)



mbb076

## 3. Ordering information

**Table 3. Ordering information**

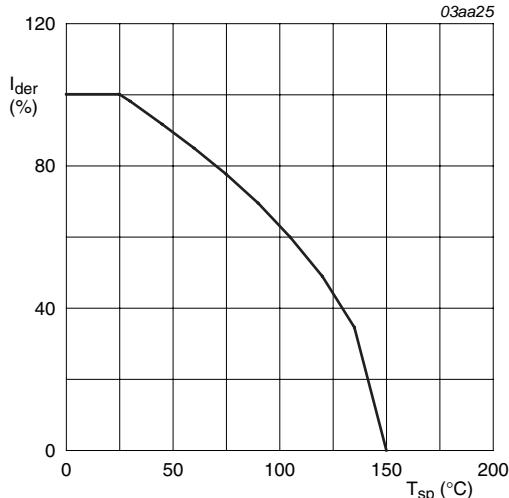
Type number	Package			Version
	Name	Description		
PHK31NQ03LT	SO8	plastic small outline package; 8 leads; body width 3.9 mm		SOT96-1

## 4. Limiting values

**Table 4. Limiting values**

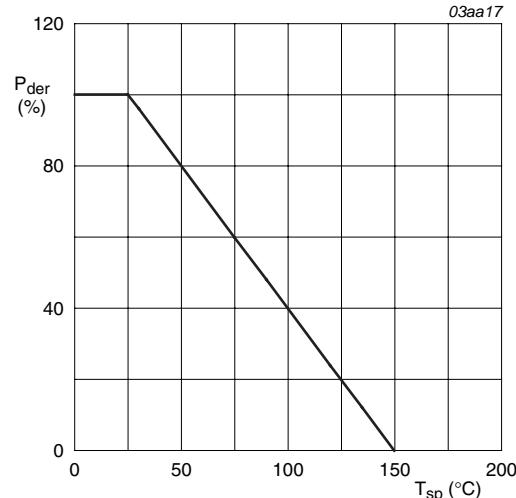
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25^\circ\text{C}; T_j \leq 150^\circ\text{C}$	-	30	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25^\circ\text{C}; T_j \leq 150^\circ\text{C}; R_{GS} = 20\text{ k}\Omega$	-	30	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$T_{sp} = 25^\circ\text{C}; V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	30.4	A
		$T_{sp} = 100^\circ\text{C}; V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a>	-	17.2	A
$I_{DM}$	peak drain current	$T_{sp} = 25^\circ\text{C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; see <a href="#">Figure 3</a>	-	121.8	A
$P_{tot}$	total power dissipation	$T_{sp} = 25^\circ\text{C}$ ; see <a href="#">Figure 2</a>	-	6.9	W
$T_{stg}$	storage temperature		-55	150	°C
$T_j$	junction temperature		-55	150	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{sp} = 25^\circ\text{C}$	-	5.7	A
$I_{SM}$	peak source current	$T_{sp} = 25^\circ\text{C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	23.1	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(init)} = 25^\circ\text{C}; I_D = 35\text{ A}; V_{sup} \leq 25\text{ V}$ ; unclamped; $t_p = 0.16\text{ ms}$ ; $R_{GS} = 50\text{ }\Omega$	-	120	mJ



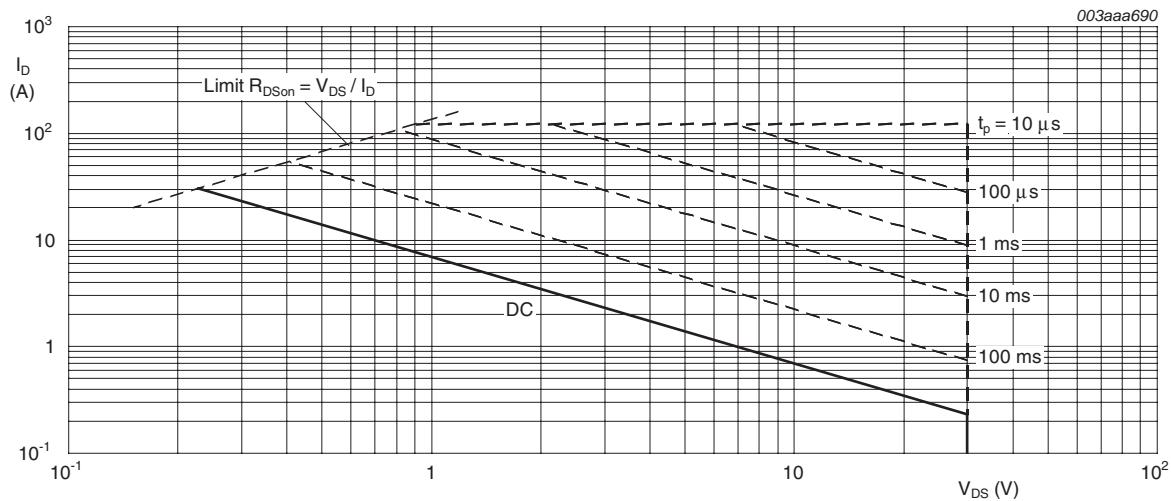
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

**Fig 1.** Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

**Fig 2.** Normalized total power dissipation as a function of solder point temperature



$T_{sp} = 25\text{ }^\circ\text{C}$ ;  $I_{DM}$  is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	18	K/W

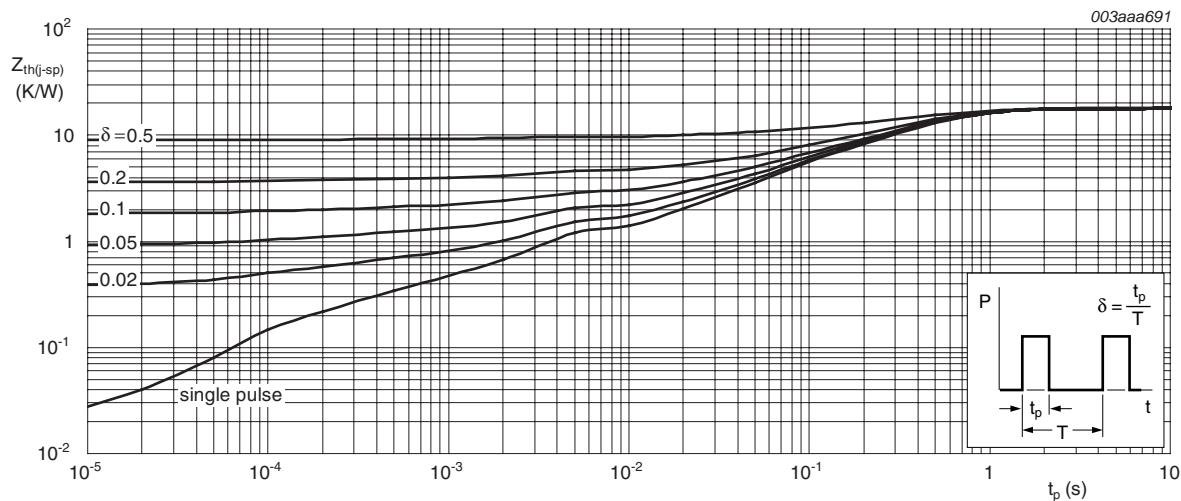


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

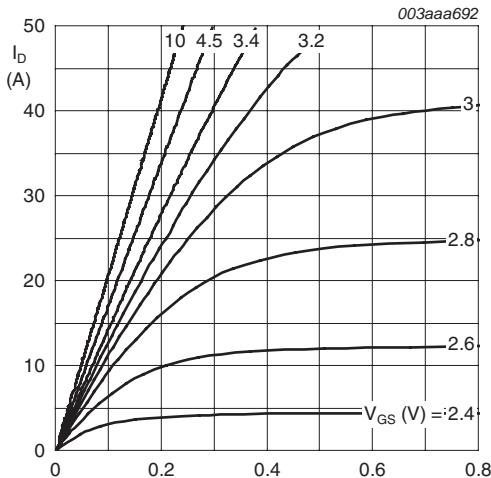
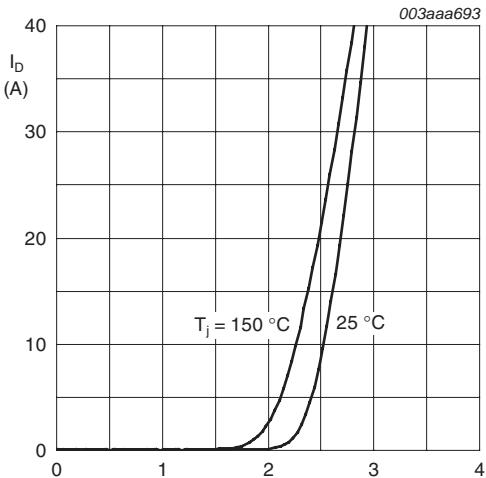
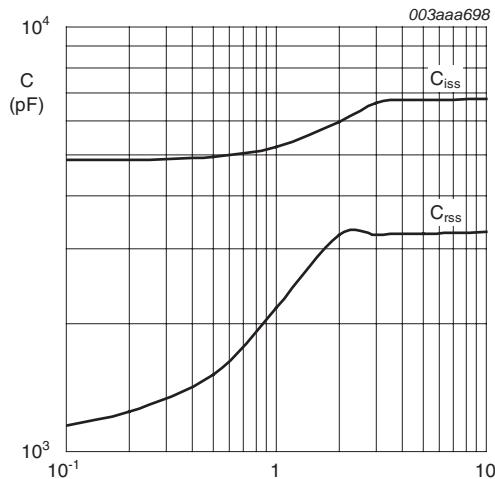
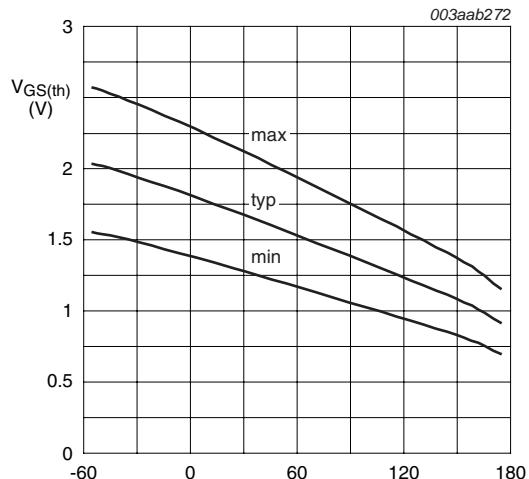
## 6. Characteristics

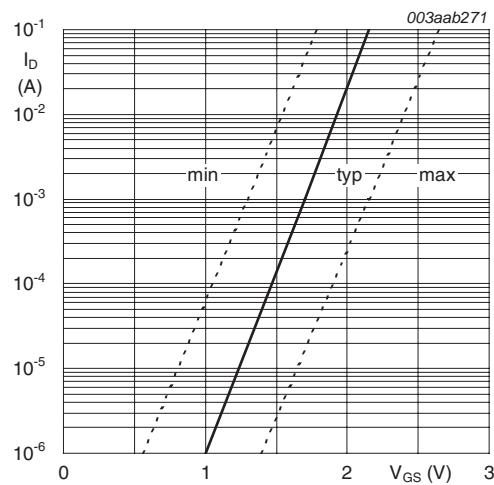
**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$ $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55^\circ C$	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25^\circ C;$ see <a href="#">Figure 8</a> ; see <a href="#">Figure 9</a> $I_D = 1 mA; V_{DS} = V_{GS}; T_j = 150^\circ C;$ see <a href="#">Figure 8</a> ; see <a href="#">Figure 9</a> $I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55^\circ C;$ see <a href="#">Figure 8</a> ; see <a href="#">Figure 9</a>	1.3	1.7	2.15	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25^\circ C$ $V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150^\circ C$	-	-	100	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25^\circ C$ $V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25^\circ C$	-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_j = 25^\circ C;$ see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a> $V_{GS} = 10 V; I_D = 25 A; T_j = 150^\circ C;$ see <a href="#">Figure 10</a> $V_{GS} = 4.5 V; I_D = 25 A; T_j = 25^\circ C;$ see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	-	3.45	4.4	$m\Omega$
$R_G$	gate resistance	$f = 1 MHz; V_{GSS(AC)} = 150 mV$	-	1.2	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V;$ see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	33	-	nC
$Q_{GS}$	gate-source charge		-	13.6	-	nC
$Q_{GS1}$	pre-threshold gate-source charge		-	6.5	-	nC
$Q_{GS2}$	post-threshold gate-source charge		-	7.1	-	nC
$Q_{GD}$	gate-drain charge		-	7.7	-	nC
$V_{GS(pi)}$	gate-source plateau voltage	$I_D = 25 A; V_{DS} = 12 V;$ see <a href="#">Figure 12</a>	-	2.85	-	V
$C_{iss}$	input capacitance	$V_{DS} = 0 V; V_{GS} = 0 V; f = 1 MHz;$ $T_j = 25^\circ C$ $V_{DS} = 12 V; V_{GS} = 0 V; f = 1 MHz;$ $T_j = 25^\circ C;$ see <a href="#">Figure 14</a>	-	4900	-	pF
$C_{oss}$	output capacitance		-	4235	-	pF
$C_{rss}$	reverse transfer capacitance		-	840	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12 V; R_L = 0.5 \Omega; V_{GS} = 4.5 V;$	-	37	-	ns
$t_r$	rise time	$R_{G(ext)} = 5.6 \Omega$	-	62	-	ns
$t_{d(off)}$	turn-off delay time		-	54	-	ns
$t_f$	fall time		-	26	-	ns

**Table 6. Characteristics ...continued**

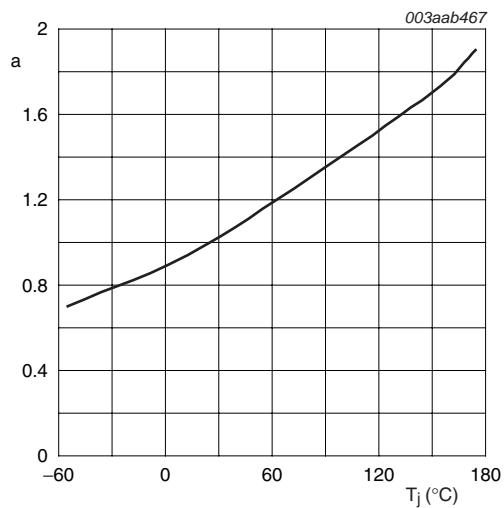
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25^\circ\text{C}$ ; see <a href="#">Figure 15</a>	-	0.94	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 30 \text{ V}$	-	52	-	ns
$Q_r$	recovered charge	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}$	-	30	-	nC

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values****Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values****Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values****Fig 8. Gate-source threshold voltage as a function of junction temperature**



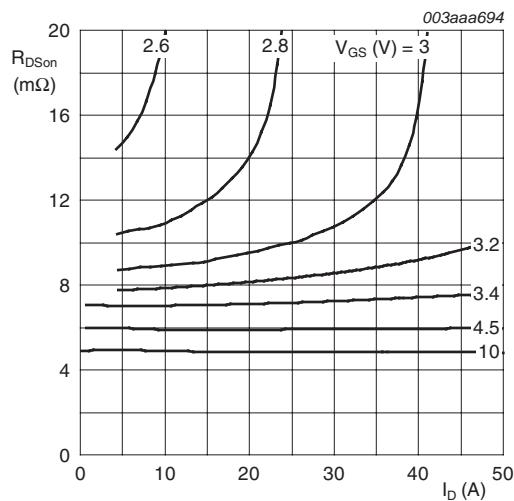
$T_f = 25^\circ C; V_{DS} = 5V$

**Fig 9. Sub-threshold drain current as a function of gate-source voltage**

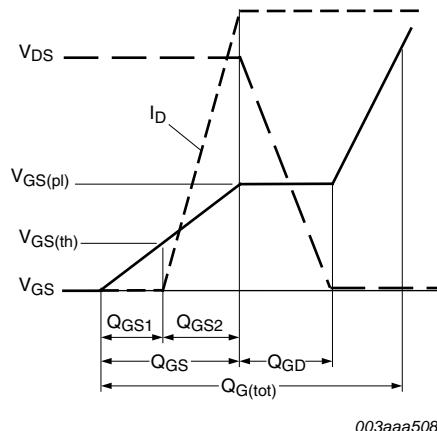


$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ C)}$$

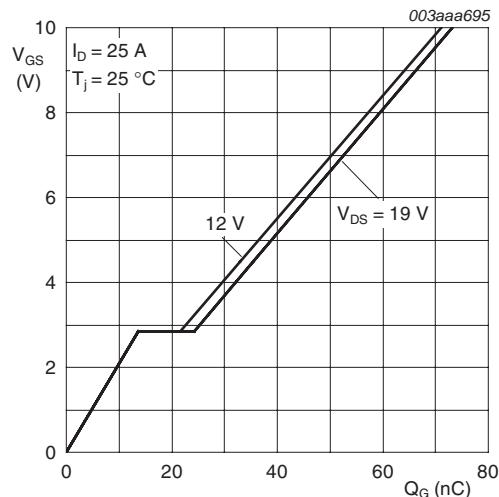
**Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature**



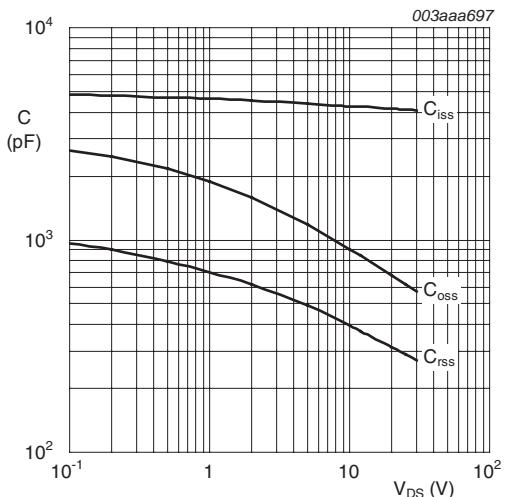
**Fig 11. Drain-source on-state resistance as a function of drain current; typical values**



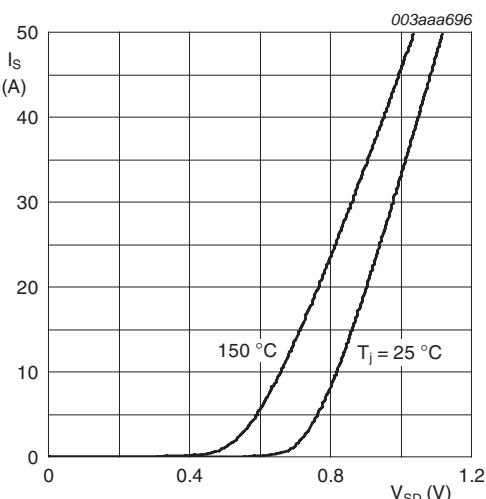
**Fig 12. Gate charge waveform definitions**



**Fig 13.** Gate-source voltage as a function of gate charge; typical values



**Fig 14.** Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

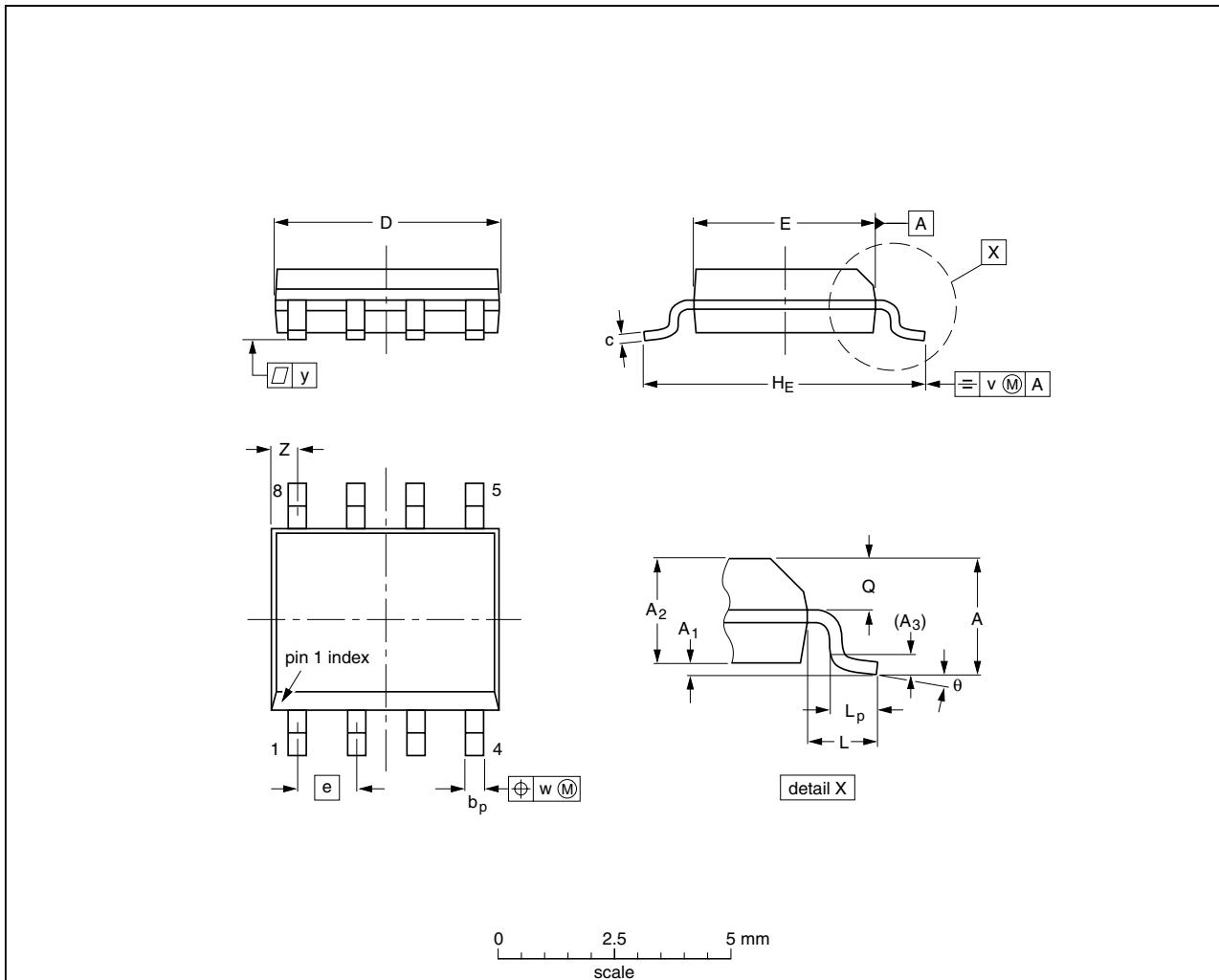


**Fig 15.** Source current as a function of source-drain voltage; typical values

## 7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75 0.10	0.25 1.45 0.36	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.004	0.010 0.049	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

**Notes**

- Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
- Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT96-1	076E03	MS-012			99-12-27 03-02-18

Fig 16. Package outline SOT96-1 (SO8)

## 8. Revision history

**Table 7. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHK31NQ03LT v.3	20110311	Product data sheet	-	PHK31NQ03LT v.2
Modifications:		• Various changes to content.		
PHK31NQ03LT v.2	20101220	Product data sheet	-	PHK31NQ03LT v.1

## 9. Legal information

### 9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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