ALPHA & OMEGA SEMICONDUCTOR

AOH3110

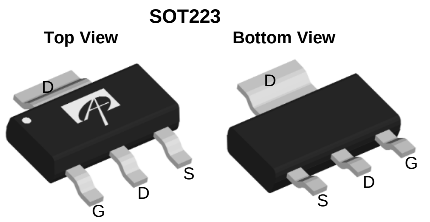
100V N-Channel MOSFET

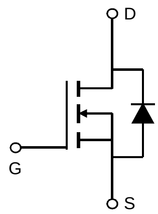
General Description

The AOH3110 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for boost converters and synchronous rectifiers for consumer, telecom, industrial power supplies and LED backlighting.

Product Summary

V_{DS}	100V
I_D (at V_{GS}=10V)	1.0A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 700mΩ
$R_{DS(ON)}$ (at V_{GS}=4.5V)	< 820mΩ





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [G]	T_A=25°C	I_D	1	A
	T_A=70°C		0.8	
Pulsed Drain Current [C]		I_{DM}	4	
Avalanche Current [C]		I_{AS}	3.5	A
Avalanche energy L=50uH [C]		E_{AS}	0.3	mJ
Power Dissipation [B]	T_A=25°C	P_D	3.1	W
	T_A=70°C		2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	33	40	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		60	75	°C/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	30	40	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V		100			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V, V_{GS}=0V				1	µA
			T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V				±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=250µA		1.7	2.3	2.9	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V		4			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=0.9A			585	700	mΩ
			T_J=125°C		1110	1340	
		V_{GS}=4.5V, I_D=0.75A			635	820	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=0.9A			2.8		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V			0.9	1.2	V
I_S	Maximum Body-Diode Continuous Current [G]					1	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=50V, f=1MHz			100		pF
C_{oss}	Output Capacitance				13		pF
C_{rss}	Reverse Transfer Capacitance				5		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		2.5	5	7.5	Ω
SWITCHING PARAMETERS							
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=50V, I_D=0.9A			2.8	6	nC
Q_g(4.5V)	Total Gate Charge				1.5	3	nC
Q_{gs}	Gate Source Charge				0.4		nC
Q_{gd}	Gate Drain Charge				0.8		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=50V, R_L=50Ω, R_{GEN}=3Ω			5		ns
t_r	Turn-On Rise Time				4		ns
$t_{D(off)}$	Turn-Off DelayTime				12		ns
t_f	Turn-Off Fall Time				5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=5.6A, dI/dt=100A/µs			52		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=5.6A, dI/dt=100A/µs			60		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating. G. The maximum current rating is package limited.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

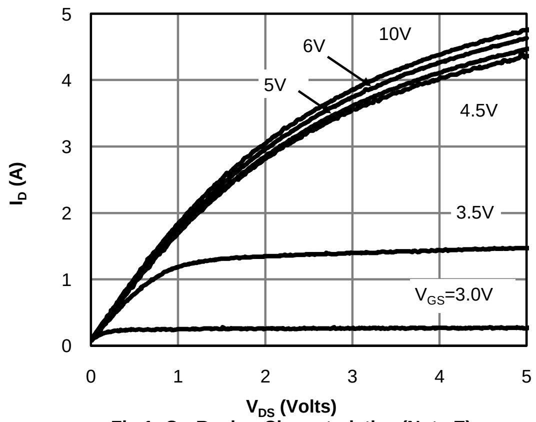


Fig 1: On-Region Characteristics (Note E)

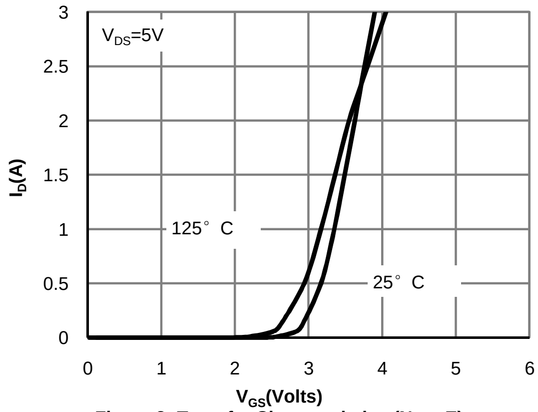


Figure 2: Transfer Characteristics (Note E)

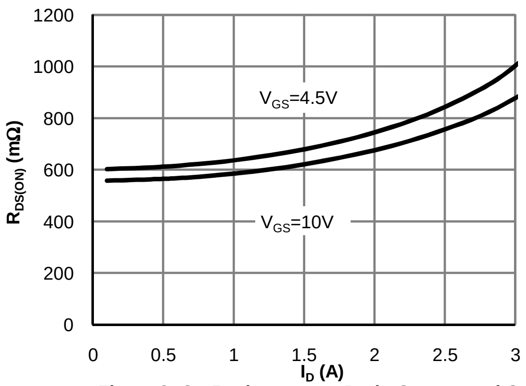


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

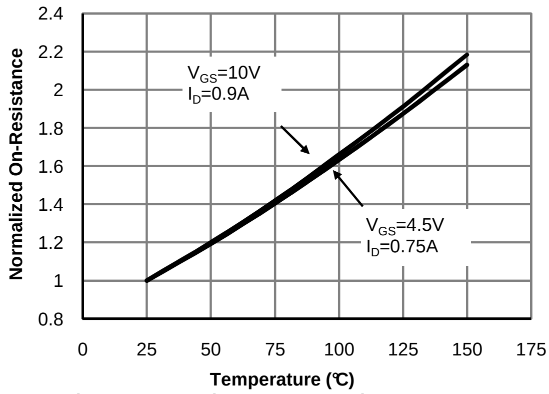


Figure 4: On-Resistance vs. Junction Temperature (Note E)

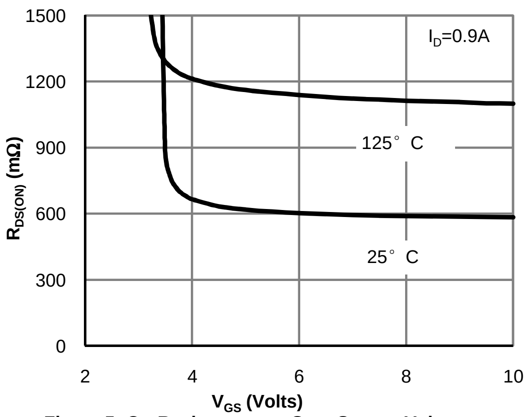


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

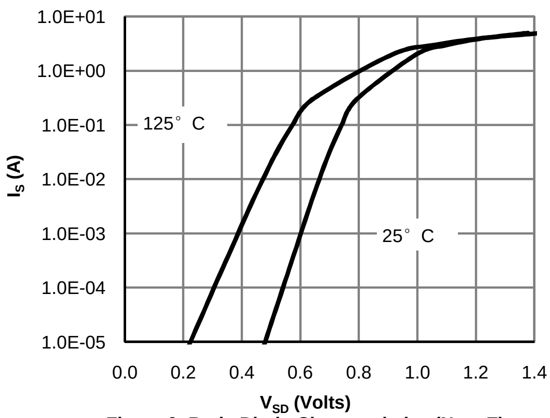


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

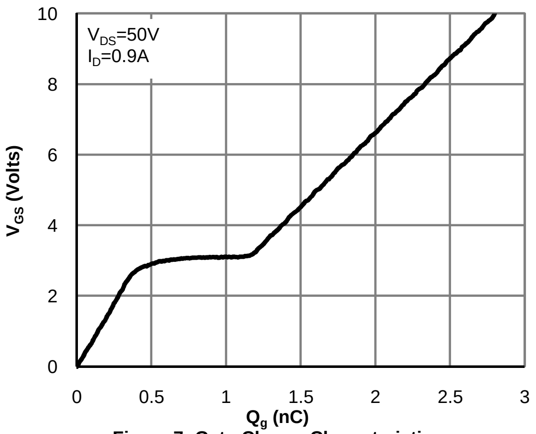


Figure 7: Gate-Charge Characteristics

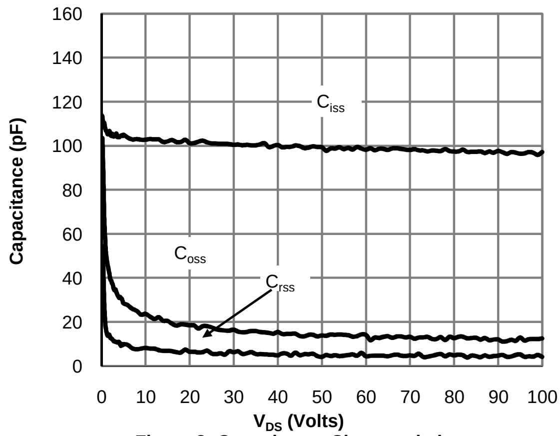


Figure 8: Capacitance Characteristics

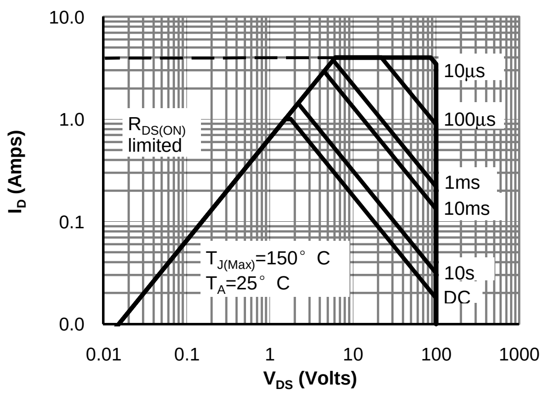


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

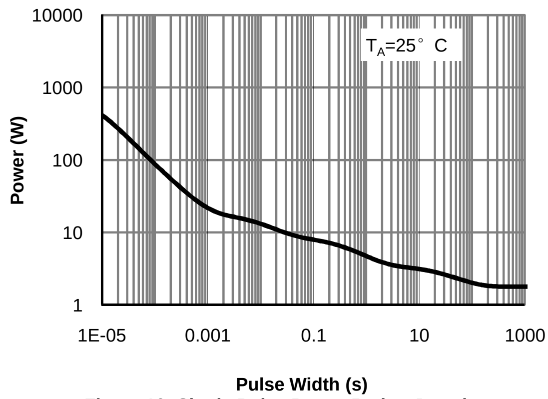


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

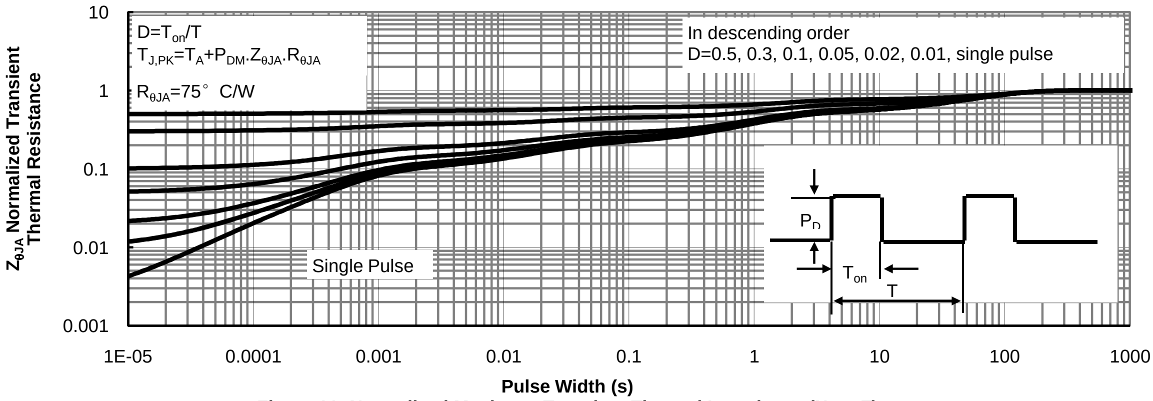
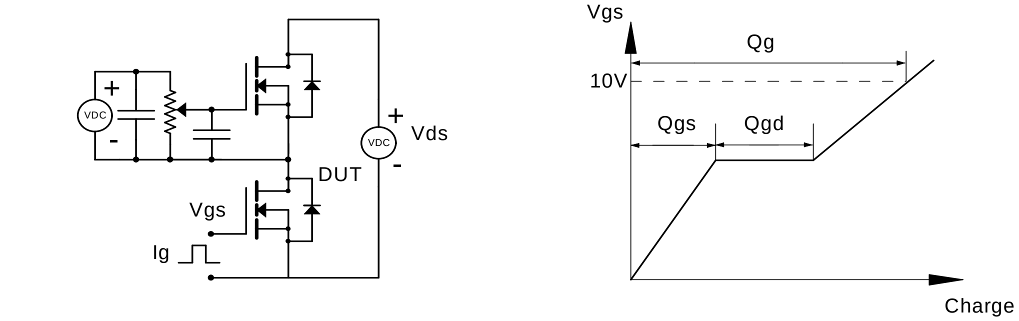
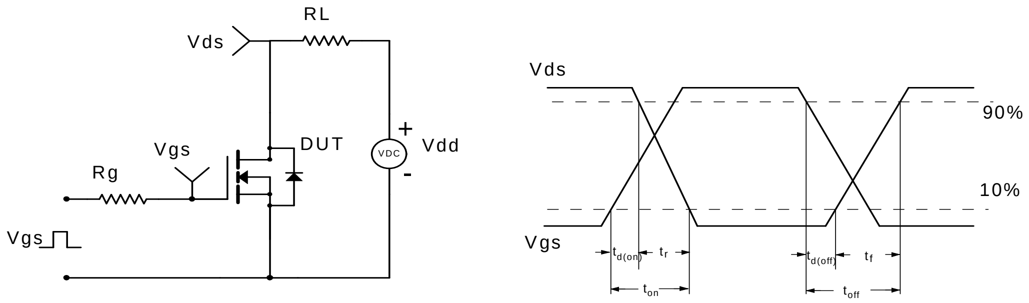


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms