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FCD900N60Z

N-Channel SuperFET® II MOSFET 600 V, 4.5 A, 900 mΩ

Features

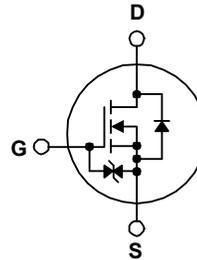
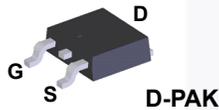
- 650 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 820\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 13\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 49\text{ pF}$)
- 100% Avalanche Tested
- ESD Improved Capacity
- RoHS Compliant

Applications

- LCD / LED / PDP TV and Monitor Lighting
- Solar Inverter
- Charger

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCD900N60Z	Unit
V_{DSS}	Drain to Source Voltage	600	V
V_{GSS}	Gate to Source Voltage	- DC	± 20
		- AC ($f > 1\text{ Hz}$)	± 30
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	4.5
		- Continuous ($T_C = 100^\circ\text{C}$)	3.5
I_{DM}	Drain Current	- Pulsed (Note 1)	13.5
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	47.5	mJ
I_{AR}	Avalanche Current (Note 1)	1	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	0.52	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	20	
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	52
		- Derate Above 25°C	0.42
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FCD900N60Z	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.4	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	100	$^\circ\text{C/W}$

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCD900N60Z	FCD900N60Z	DPAK	Tape and Reel	330 mm	16 mm	2500 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 25^\circ\text{C}$	600	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 150^\circ\text{C}$	650	-	-	
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, Referenced to 25°C	-	0.67	-	$\text{V}/^\circ\text{C}$
BV_{DS}	Drain to Source Avalanche Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 4.5\text{ A}$	-	700	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}$	-	-	5	μA
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	-	-	20	
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	10	μA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	-	-	-10	μA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	2.5	-	3.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 2.3\text{ A}$	-	0.82	0.90	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 2.3\text{ A}$	-	4.6	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	543	720	μF
C_{oss}	Output Capacitance		-	400	530	μF
C_{riss}	Reverse Transfer Capacitance		-	20	30	μF
C_{oss}	Output Capacitance	$V_{DS} = 380\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	11	-	μF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$	-	49	-	μF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380\text{ V}, I_D = 2.3\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)	-	13	17	nC
Q_{gs}	Gate to Source Gate Charge		-	2.3	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	4.8	-	nC
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$	-	2.4	-	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{ V}, I_D = 2.3\text{ A}, V_{GS} = 10\text{ V}, R_G = 4.7\text{ }\Omega$ (Note 4)	-	10.9	32	ns
t_r	Turn-On Rise Time		-	5.3	21	ns
$t_{d(off)}$	Turn-Off Delay Time		-	33.6	77	ns
t_f	Turn-Off Fall Time		-	11.9	34	ns

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	4.5	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	13.5	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 2.3\text{ A}$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 2.3\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$	-	156	-	ns
Q_{rr}	Reverse Recovery Charge		-	1.3	-	μC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $I_{AS} = 1\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 2.3\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

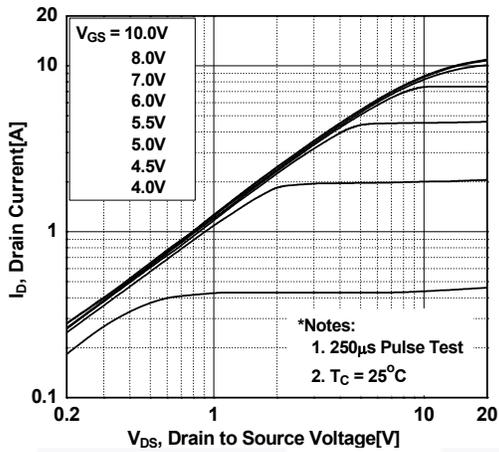


Figure 2. Transfer Characteristics

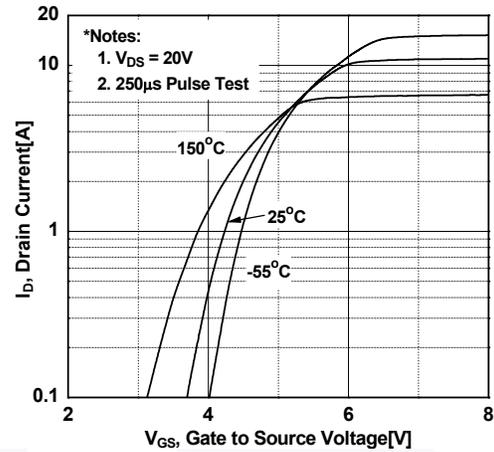


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

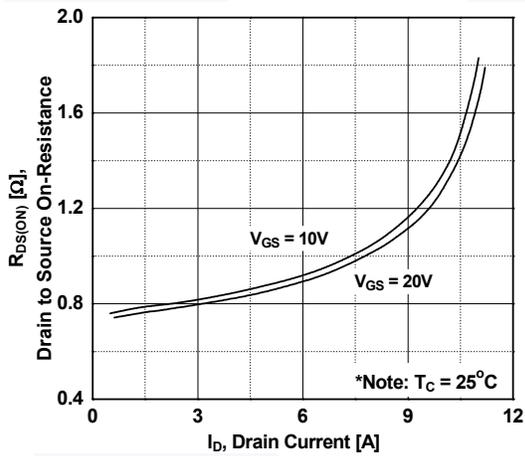


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

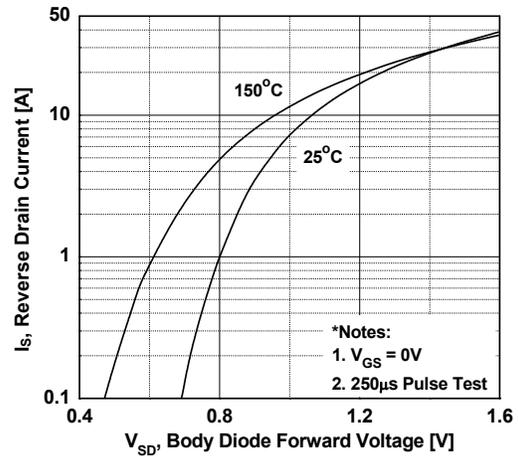


Figure 5. Capacitance Characteristics

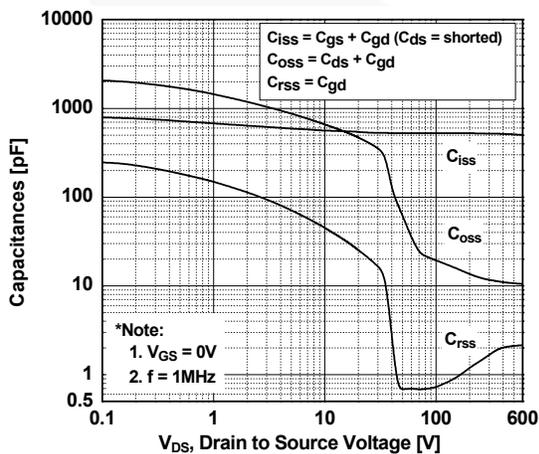
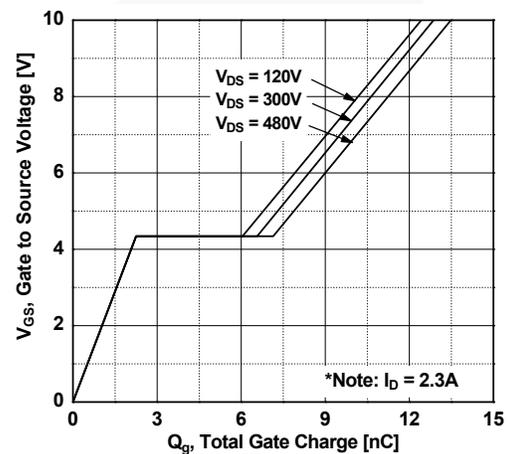


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

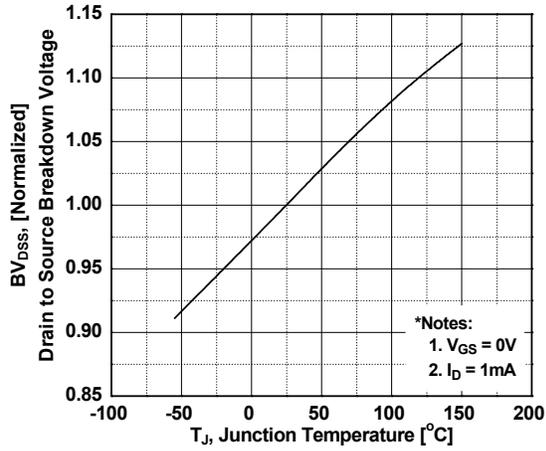


Figure 8. On-Resistance Variation vs. Temperature

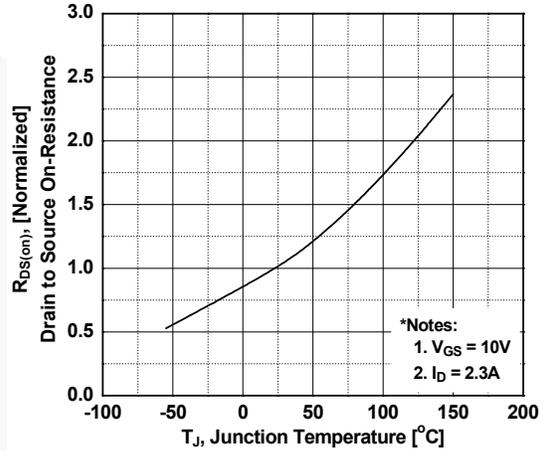


Figure 9. Maximum Safe Operating Area

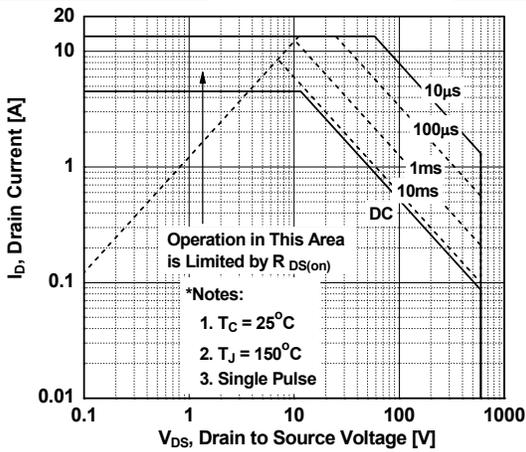


Figure 10. Maximum Drain Current vs. Case Temperature

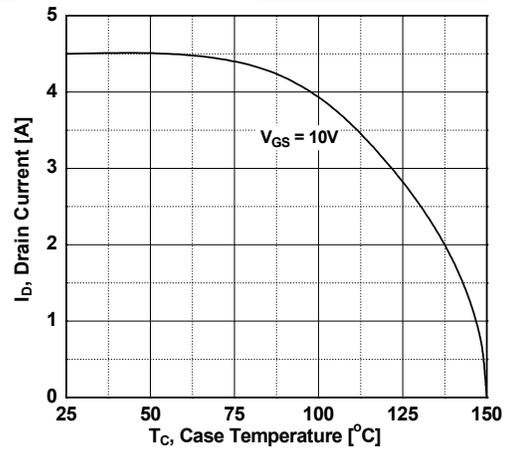
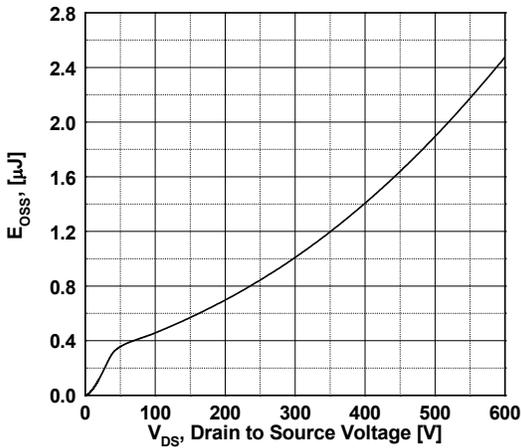
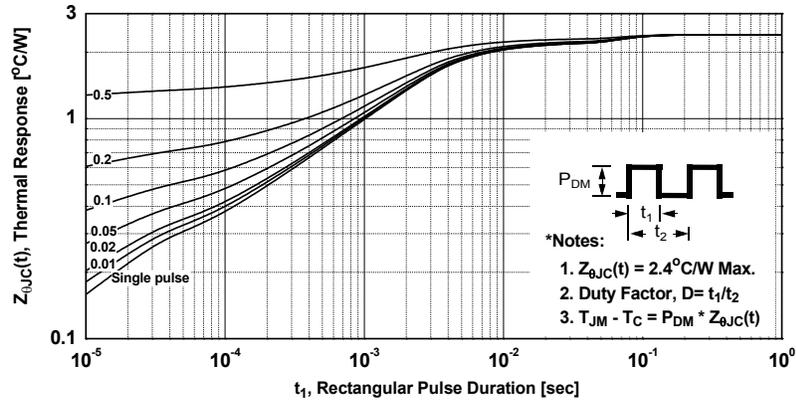


Figure 11. E_oss vs. Drain to Source Voltage



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



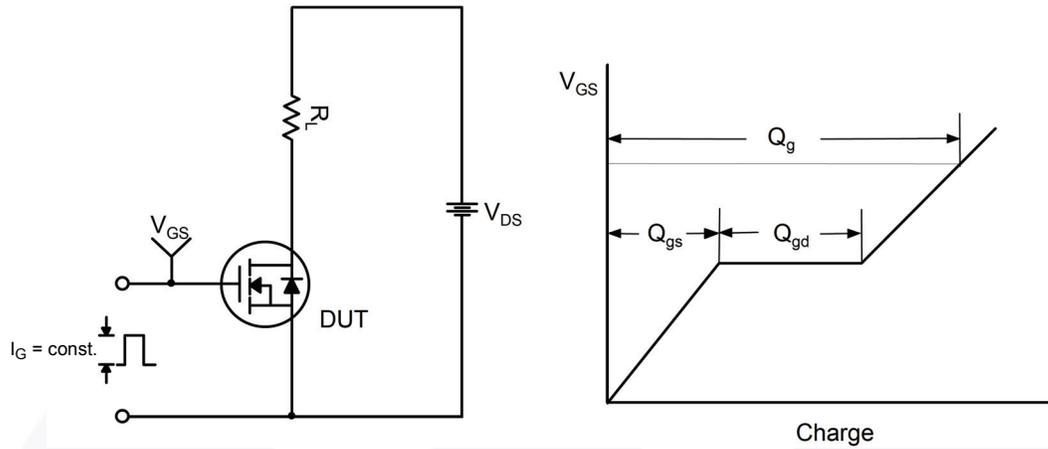


Figure 13. Gate Charge Test Circuit & Waveform

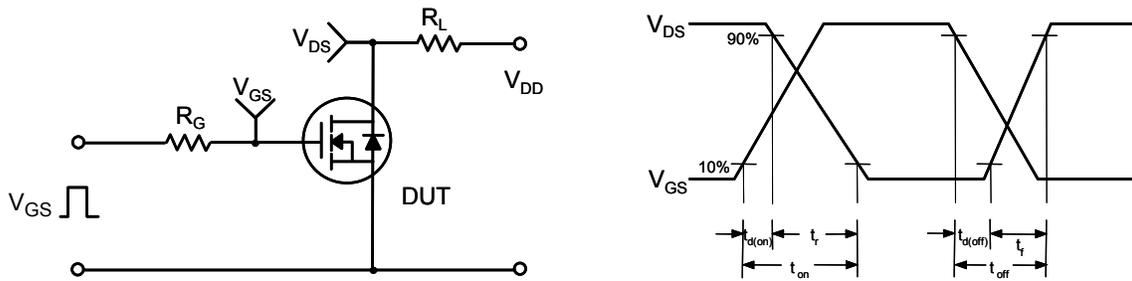


Figure 14. Resistive Switching Test Circuit & Waveforms

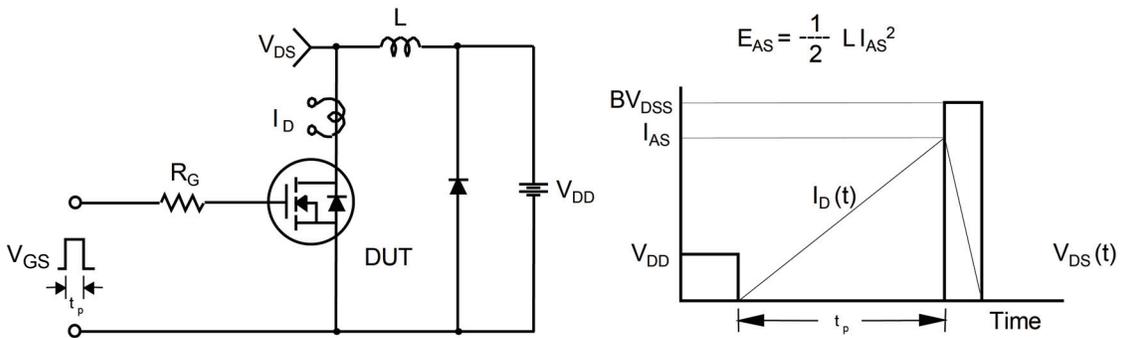


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

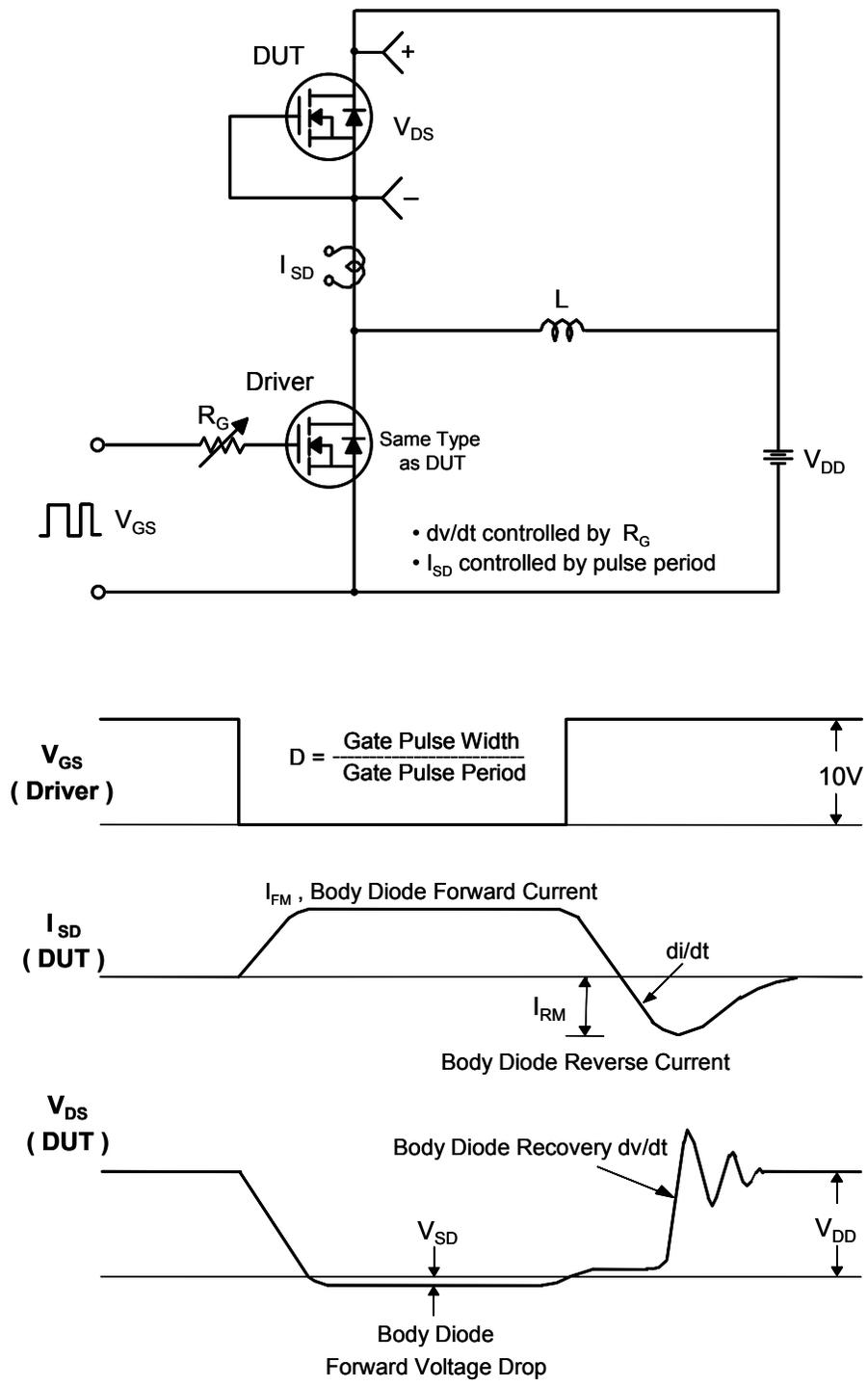
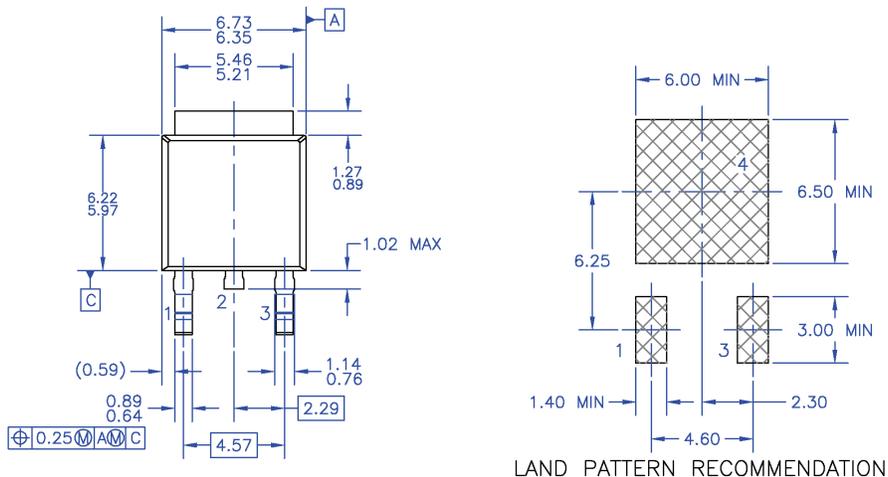


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
 - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC351A STD TO220P1003X238-3N.
 - H) DRAWING NUMBER AND REVISION: MKT-T0252A03REV8

Figure 17. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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