OptiMOS™2 Power-Transistor

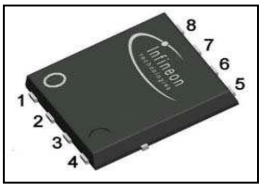
Features

- Fast switching MOSFET for SMPS
- Optimized technology for notebook DC/DC converters
- Qualified according to JEDEC[1] for target applications
- Logic level / N-channel
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- Avalanche rated; dv/dt rated
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product Summary

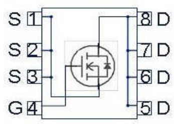
V_{DS}	30	V
$R_{DS(on),max}$	4.2	mΩ
I_D	95	A

PG-TDSON-8



RoHS

Halogen-Free



Type	Package	Marking
BSC042N03S G	PG-TDSON-8	42N03S

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C	95	A
		T_C=100 °C	60	
		T_A=25 °C, R_{thJA}=45 K/W[2)]	20	
Pulsed drain current	$I_{D,pulse}$	T_C=25 °C[3)]	200	
Avalanche energy, single pulse	E_{AS}	I_D=50 A, R_{GS}=25 Ω	280	mJ
Reverse diode d*v*/d*t*	d*v*/d*t*	I_D=50 A, V_{DS}=24 V, d*i*/d*t*=200 A/µs, $T_{j,max}$=150 °C	6	kV/µs
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	62.5	W
		T_A=25 °C, R_{thJA}=45 K/W[2)]	2.8	
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}	bottom	-	-	2	K/W
		top			18	
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint	-	-	62	
		6 cm^2 cooling area[2)]	-	-	45	

Electrical characteristics, at T_j=25 °C, unless otherwise specified

Static characteristics

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=50 µA	1.2	1.6	2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=30 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=30 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=50 A	-	5.2	6.5	mΩ
		V_{GS}=10 V, I_D=50 A	-	3.5	4.2	
Gate resistance	R_G		0.4	0.9	1.8	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=50 A	49	98	-	S

[1)] J-STD20 and JESD22

[2)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

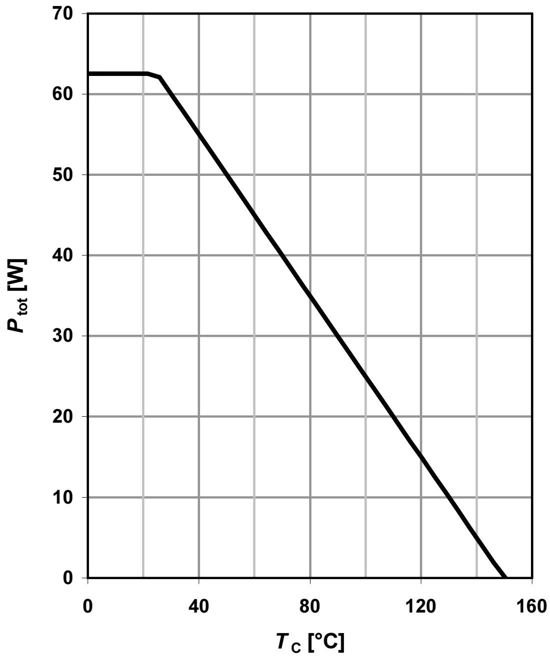
[3)] See figure 3

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz	-	2750	3660	pF
Output capacitance	C_{oss}		-	980	1300	
Reverse transfer capacitance	C_{rss}		-	130	195	
Turn-on delay time	$t_{d(on)}$	V_{DD}=15 V, V_{GS}=10 V, I_D=25 A, R_G=2.7 Ω	-	6.8	10	ns
Rise time	t_r		-	5.8	8.7	
Turn-off delay time	$t_{d(off)}$		-	27	41	
Fall time	t_f		-	4.6	6.9	
Gate Charge Characteristics[4)]						
Gate to source charge	Q_{gs}	V_{DD}=15 V, I_D=25 A, V_{GS}=0 to 5 V	-	8.3	11	nC
Gate charge at threshold	$Q_{g(th)}$		-	4.4	5.9	
Gate to drain charge	Q_{gd}		-	5.3	8.0	
Switching charge	Q_{sw}		-	9.2	13	
Gate charge total	Q_g		-	21	28	
Gate plateau voltage	$V_{plateau}$		-	3.0	-	V
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 5 V	-	19	25	nC
Output charge	Q_{oss}	V_{DD}=15 V, V_{GS}=0 V	-	23	31	
Reverse Diode						
Diode continous forward current	I_S	T_C=25 °C	-	-	50	A
Diode pulse current	$I_{S,pulse}$		-	-	200	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=50 A, T_j=25 °C	-	0.85	1	V
Reverse recovery charge	Q_{rr}	V_R=15 V, I_F=I_S, di_F/dt=400 A/µs	-	-	12	nC

[4)] See figure 16 for gate charge parameter definition

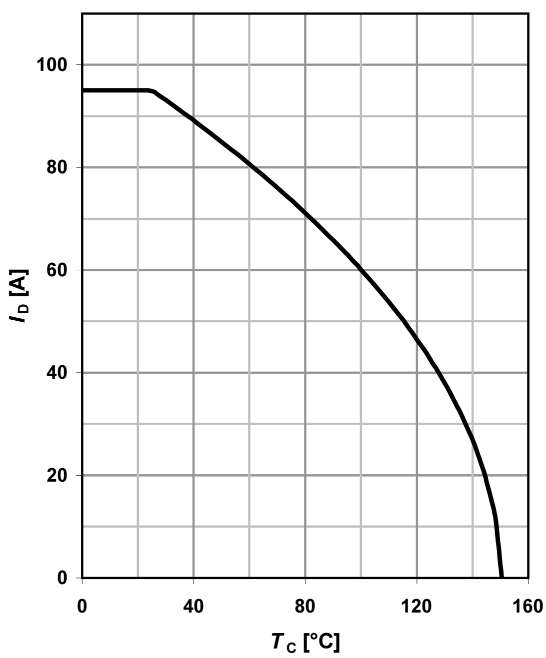
1 Power dissipation

P_{tot}=f(T_C)



2 Drain current

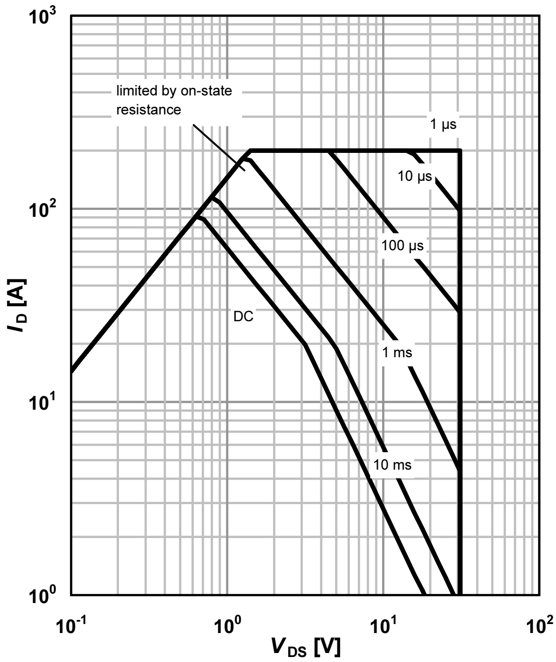
I_D=f(T_C); V_{GS}≥10 V



3 Safe operating area

I_D=f(V_{DS}); T_C=25 °C; D=0

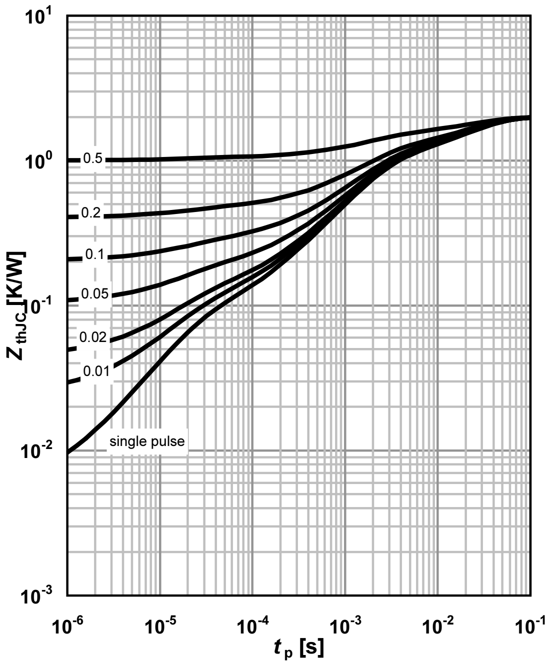
parameter: t_p



4 Max. transient thermal impedance

Z_{thJC}=f(t_p)

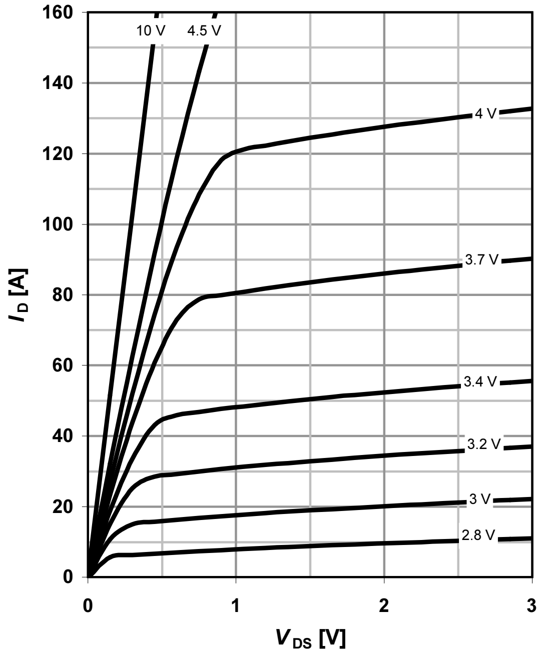
parameter: D=t_p/T



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

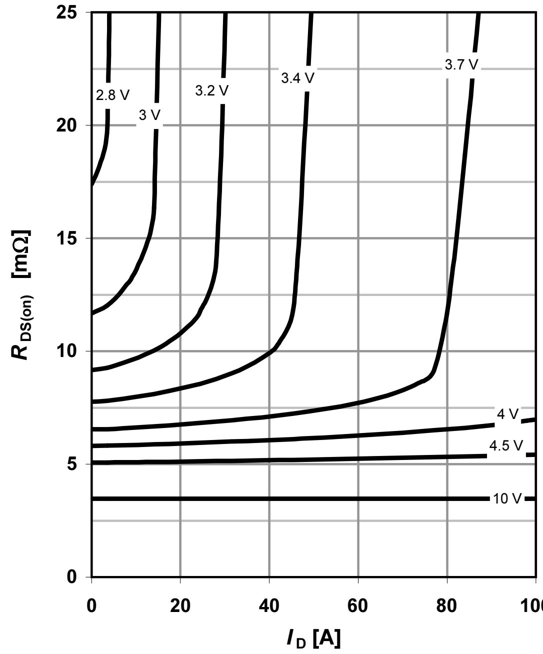
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

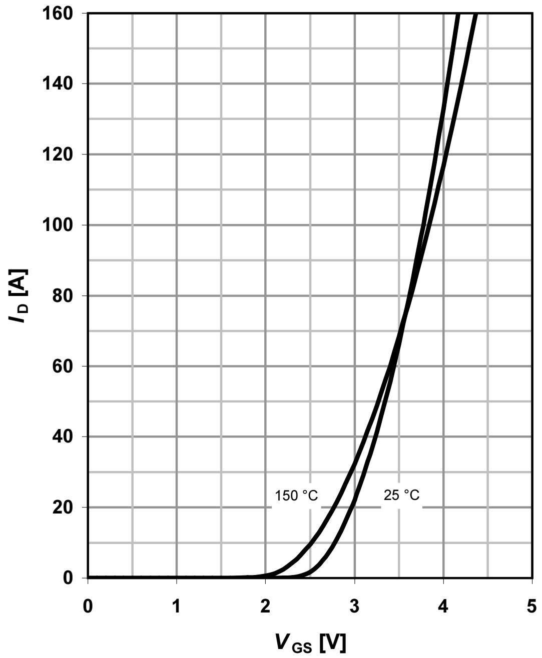
parameter: V_{GS}



7 Typ. transfer characteristics

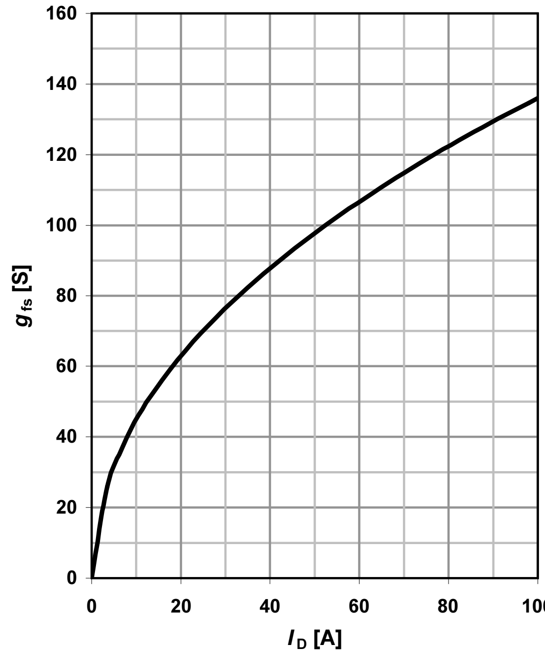
I_D=f(V_{GS}); $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



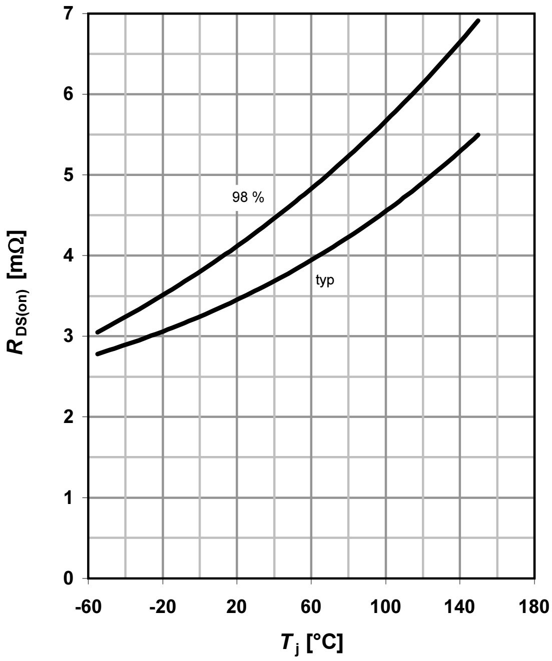
8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



9 Drain-source on-state resistance

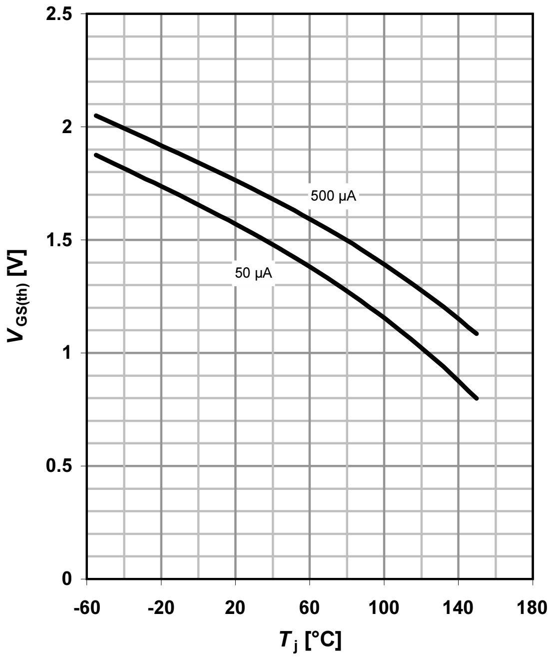
$R_{DS(on)}$=f(T_j); I_D=50 A; V_{GS}=10 V



10 Typ. gate threshold voltage

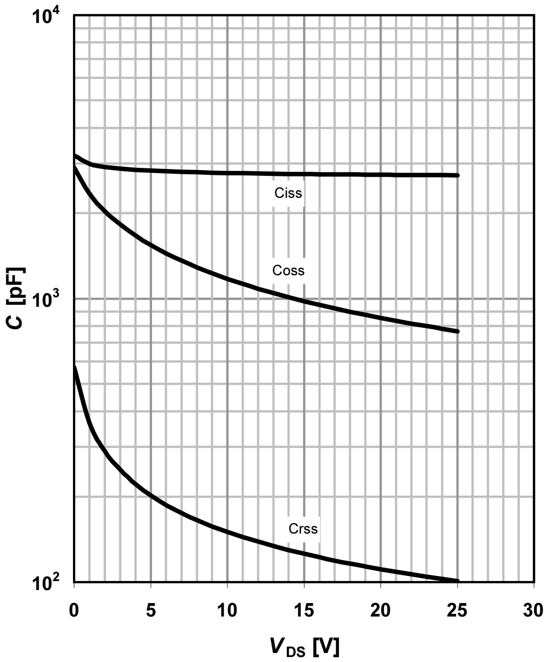
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}

parameter: I_D



11 Typ. capacitances

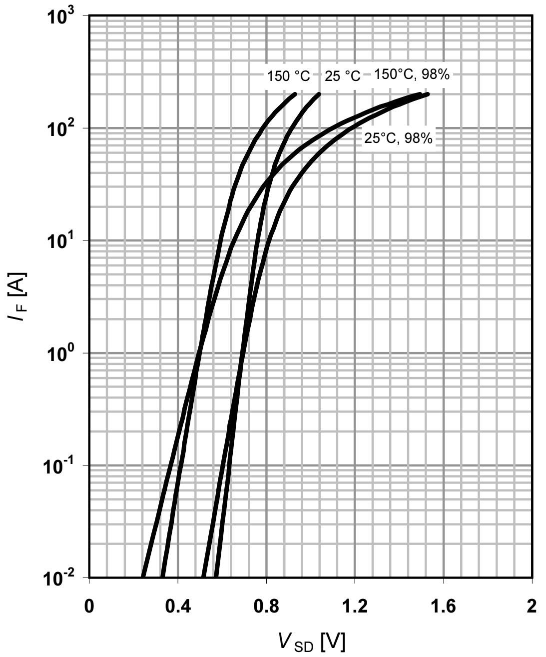
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

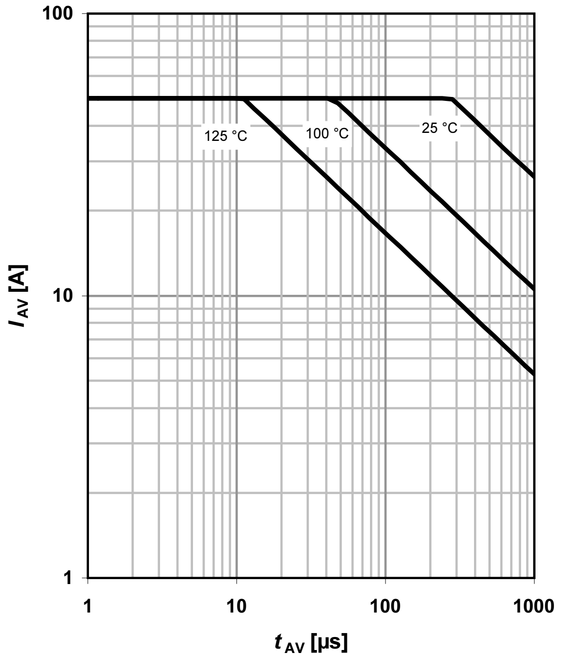
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

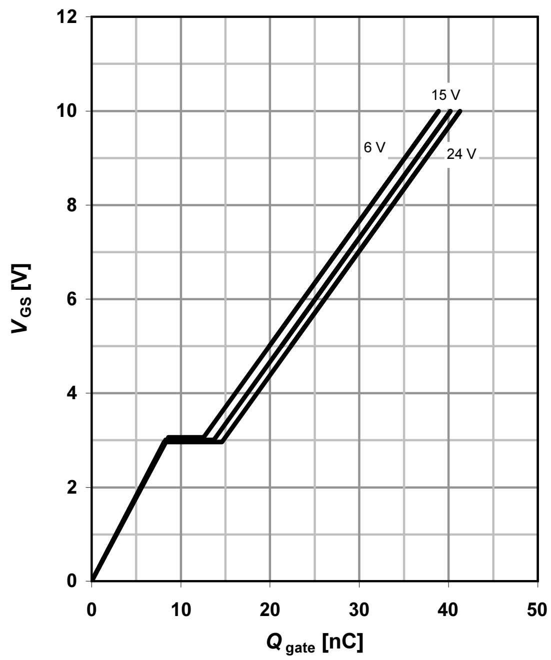
parameter: $T_{j(start)}$



14 Typ. gate charge

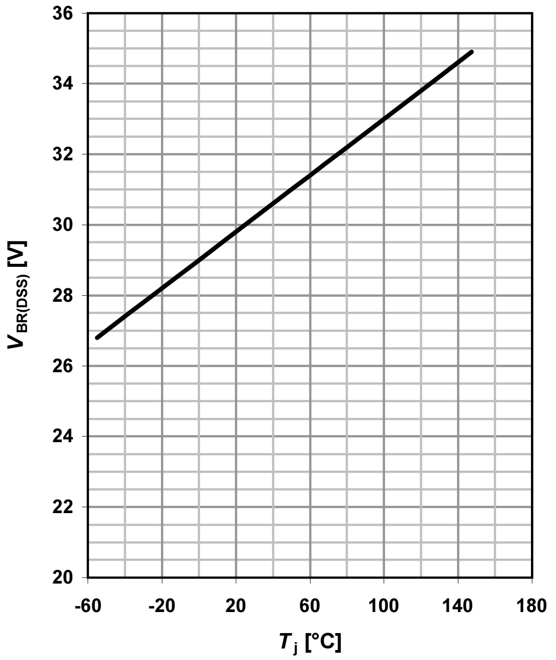
V_{GS}=f(Q_{gate}); I_D=25 A pulsed

parameter: V_{DD}

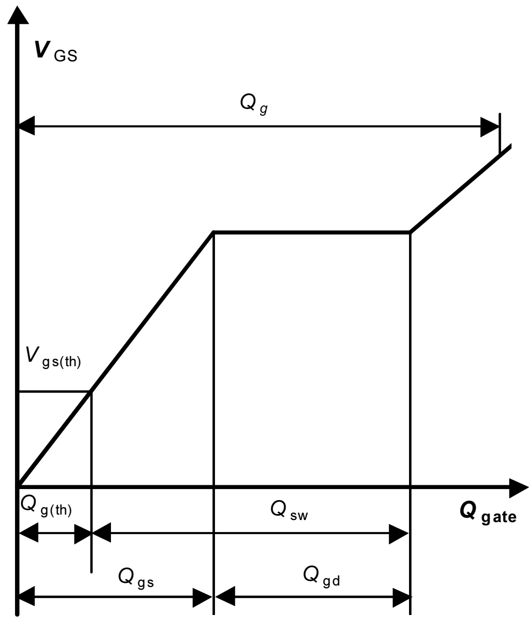


15 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=1 mA

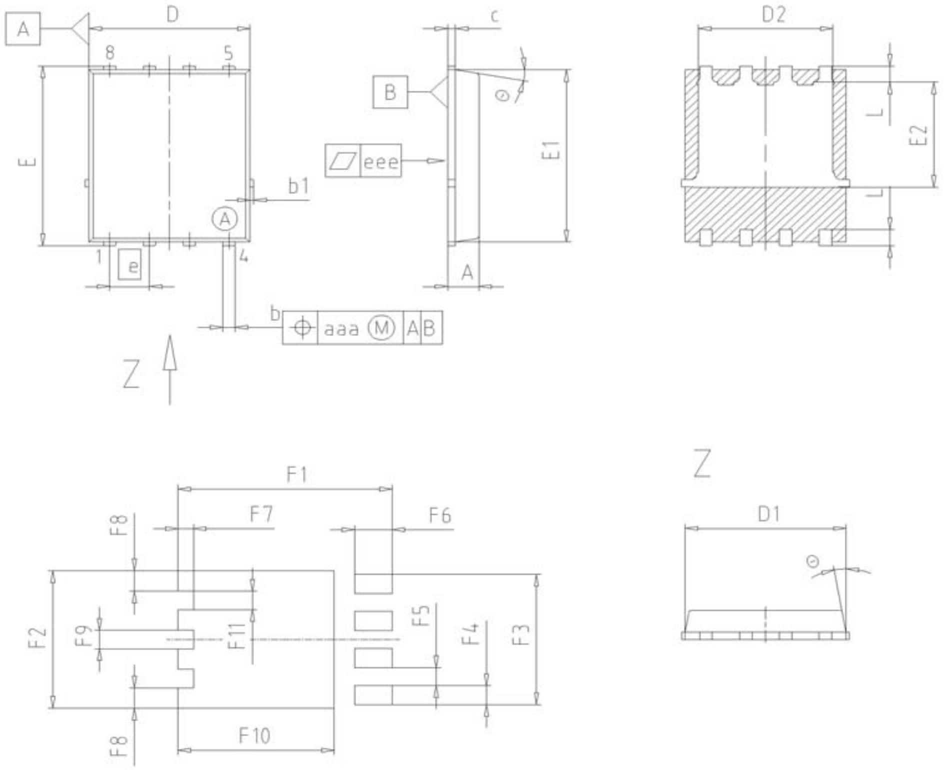


16 Gate charge waveforms



Package Outline **PG-TDSON-8**

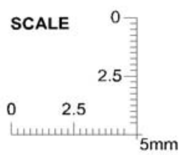
: Outline



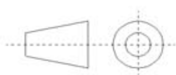
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.34	0.54	0.013	0.021
b1	0.02	0.22	0.001	0.008
c	0.15	0.35	0.006	0.014
D=D1	4.95	5.35	0.195	0.211
D2	4.20	4.40	0.165	0.173
E	5.95	6.35	0.234	0.250
E1	5.70	6.10	0.224	0.240
E2	3.40	3.80	0.134	0.150
e	1.27		0.050	
N	8		8	
L	0.45	0.65	0.018	0.026
□	8.5°	11.5°	8.5°	11.5°
aaa	0.25		0.010	
eee	0.05		0.002	
F1	6.75	6.95	0.266	0.274
F2	4.60	4.80	0.181	0.189
F3	4.36	4.56	0.172	0.180
F4	0.55	0.75	0.022	0.030
F5	0.52	0.72	0.020	0.028
F6	1.10	1.30	0.043	0.051
F7	0.40	0.60	0.016	0.024
F8	0.60	0.80	0.024	0.031
F9	0.53	0.73	0.021	0.029
F10	4.90	5.10	0.193	0.201
F11	0.53	0.73	0.021	0.029

DOCUMENT NO.
Z8B00003332

SCALE



EUROPEAN PROJECTION



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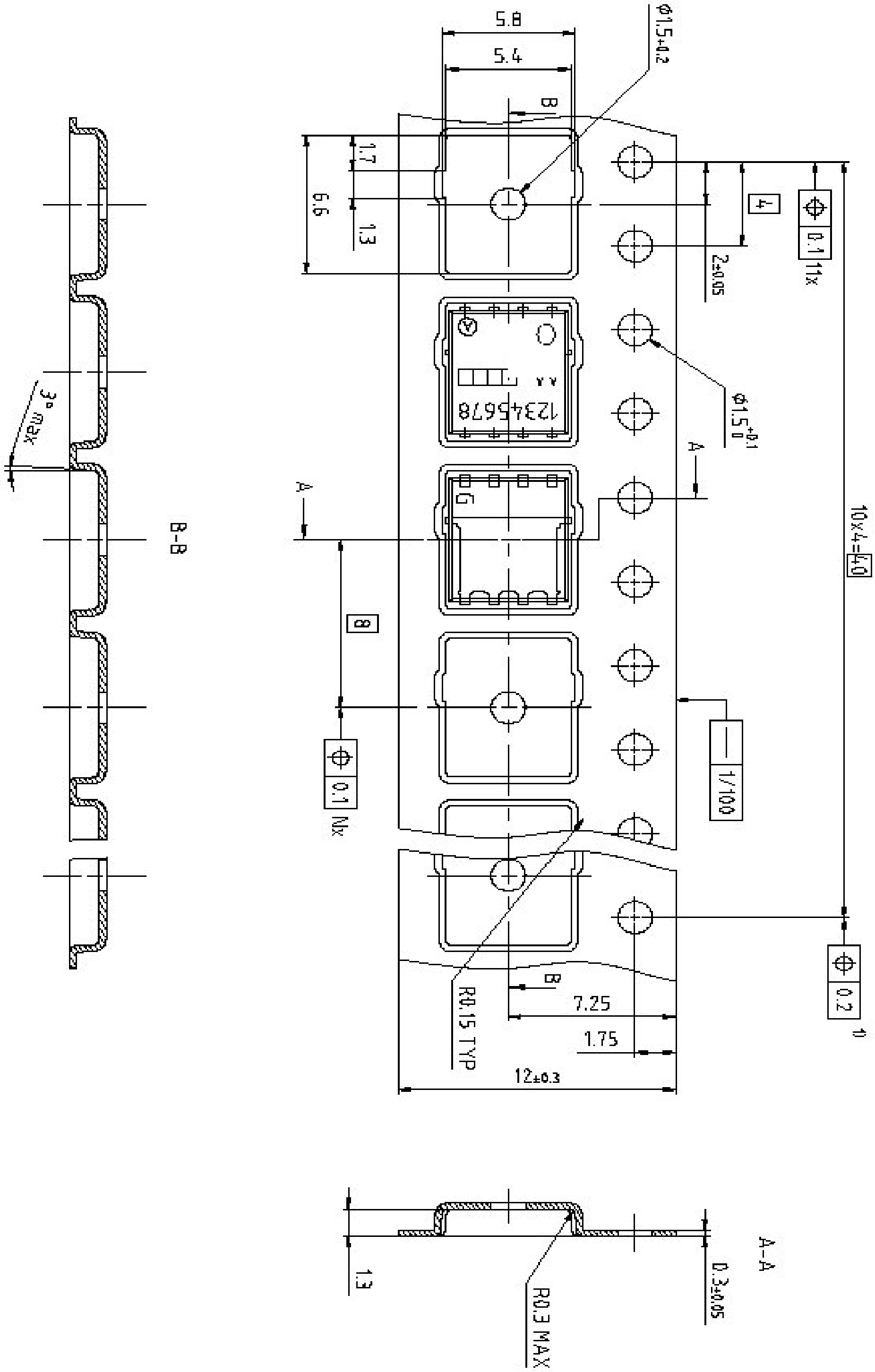
03

Package Outline

PG-TDSON-8: Tape



Dimensions in mm

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