

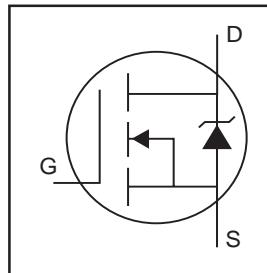
# International **IR** Rectifier

PD-91843A

## IRLBL1304

HEXFET® Power MOSFET

- >1mm lower profile than D<sup>2</sup>Pak
- Same footprint as D<sup>2</sup>pak
- Logic Level Gate
- Surface mount
- Ultra Low On-Resistance
- Fully Avalanche Rated
- 50% greater current in typ. application condition vs. D<sup>2</sup>Pak



$V_{DSS} = 40V$   
 $R_{DS(on)} = 0.0045\Omega$   
 $I_D = 185A^{\circ}$

### Description

The HEXFET® MOSFET is the most popular power MOSFET in the world.

This particular HEXFET® MOSFET is in the SuperD<sup>2</sup>Pak™ and has the same outline and pinout as the standard D<sup>2</sup>Pak but has increased current handling capability and >1mm lower profile. This makes it ideal to reduce component count in multiparallel D<sup>2</sup>Pak operation, reduce system power dissipation or upgrade existing design.

This package has also been designed to meet automotive qualification standard Q101 and can be used with normal surface mounting equipment and has the same temperature profile and recommendations as the commonly used D<sup>2</sup>Pak.



Super-D<sup>2</sup>Pak™

### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{\circ}$	185, pkg limited to 95A*	
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{\circ}$	130, pkg limited to 95A*	A
$I_{DM}$	Pulsed Drain Current $\textcircled{1}\textcircled{6}$	740	
$P_D @ T_C = 25^\circ C$	Power Dissipation	300	W
	Linear Derating Factor	2.0	W/ $^\circ C$
$V_{GS}$	Gate-to-Source Voltage	$\pm 16$	V
$E_{AS}$	Single Pulse Avalanche Energy $\textcircled{2}\textcircled{6}$	1160	mJ
$I_{AR}$	Avalanche Current $\textcircled{1}$	100	A
$E_{AR}$	Repetitive Avalanche Energy $\textcircled{1}$	30	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ $\textcircled{3}\textcircled{6}$	5.0	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	$^\circ C$
	Soldering Temperature, for 10 seconds	260 (1.6mm from case )	

### Thermal Resistance

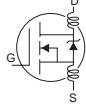
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.50	W
$R_{\theta JA}$	Junction-to-Ambient	—	40	

\* Current capability in normal application, see Fig.9.

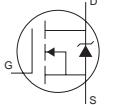
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## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

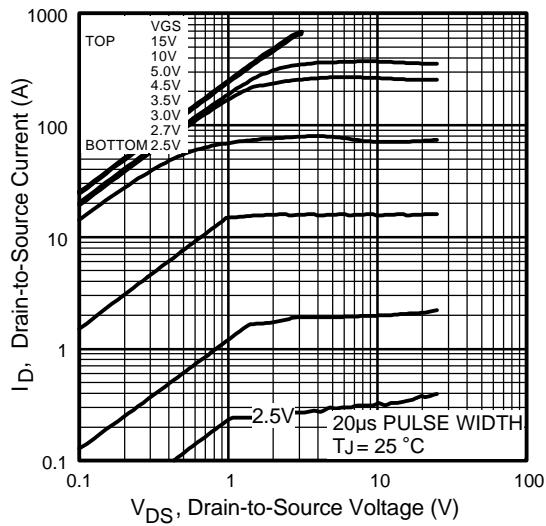
	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{\text{GS}} = 0\text{V}$ , $I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}/\Delta T_J}$	Breakdown Voltage Temp. Coefficient	—	0.043	—	$\text{V}^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$ ⑥
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	—	0.0045	$\Omega$	$V_{\text{GS}} = 10\text{V}$ , $I_D = 110\text{A}$ ④
		—	—	0.0065		$V_{\text{GS}} = 4.5\text{V}$ , $I_D = 93$ ④
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	1.0	—	—	V	$V_{\text{DS}} = V_{\text{GS}}$ , $I_D = 250\mu\text{A}$
$g_f$	Forward Transconductance	120	—	—	S	$V_{\text{DS}} = 25\text{V}$ , $I_D = 110\text{A}$ ⑥
$I_{\text{DSS}}$	Drain-to-Source Leakage Current	—	—	25	$\mu\text{A}$	$V_{\text{DS}} = 40\text{V}$ , $V_{\text{GS}} = 0\text{V}$
		—	—	250		$V_{\text{DS}} = 32\text{V}$ , $V_{\text{GS}} = 0\text{V}$ , $T_J = 150^\circ\text{C}$
$I_{\text{GSS}}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{\text{GS}} = 16\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{\text{GS}} = -16\text{V}$
$Q_g$	Total Gate Charge	—	—	140	nC	$I_D = 110\text{A}$
$Q_{\text{gs}}$	Gate-to-Source Charge	—	—	39		$V_{\text{DS}} = 32\text{V}$
$Q_{\text{gd}}$	Gate-to-Drain ("Miller") Charge	—	—	79		$V_{\text{GS}} = 4.5\text{V}$ , See Fig. 6 and 13 ④⑥
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	—	21	—		$V_{\text{DD}} = 20\text{V}$
$t_r$	Rise Time	—	350	—		$I_D = 110\text{A}$
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	—	45	—		$R_G = 0.9\Omega$
$t_f$	Fall Time	—	103	—		$R_D = 0.18\Omega$ , See Fig. 10 ④⑥
$L_D$	Internal Drain Inductance	—	2.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	5.0	—		
$C_{\text{iss}}$	Input Capacitance	—	7660	—	pF	$V_{\text{GS}} = 0\text{V}$
$C_{\text{oss}}$	Output Capacitance	—	2150	—		$V_{\text{DS}} = 25\text{V}$
$C_{\text{rss}}$	Reverse Transfer Capacitance	—	460	—		$f = 1.0\text{MHz}$ , See Fig. 5⑥

## Source-Drain Ratings and Characteristics

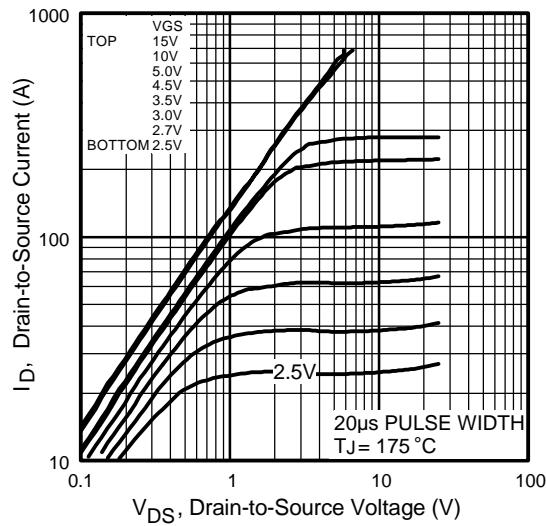
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	185⑤	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{\text{SM}}$	Pulsed Source Current (Body Diode) ①	—	—	740		
$V_{\text{SD}}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$ , $I_S = 110\text{A}$ , $V_{\text{GS}} = 0\text{V}$ ④
$t_{\text{rr}}$	Reverse Recovery Time	—	100	150	ns	$T_J = 25^\circ\text{C}$ , $I_F = 110\text{A}$
$Q_{\text{rr}}$	Reverse Recovery Charge	—	250	380	nC	$dI/dt = 100\text{A}/\mu\text{s}$ ④⑥
$t_{\text{on}}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

### Notes:

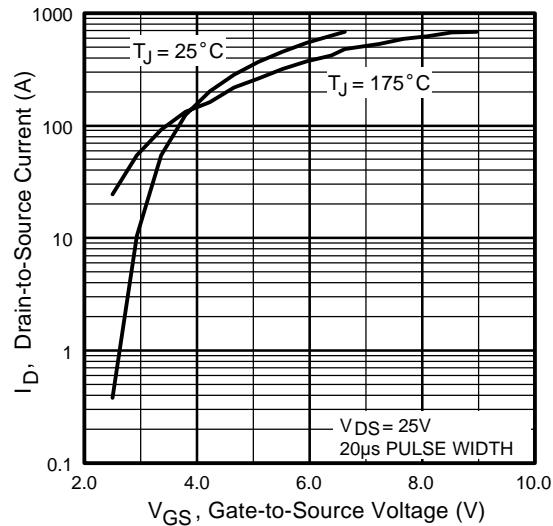
- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 230\mu\text{H}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 100\text{A}$ . (See Figure 12)
- ③  $I_{SD} \leq 110\text{A}$ ,  $dI/dt \leq 170\text{A}/\mu\text{s}$ ,  $V_{\text{DD}} \leq V_{(\text{BR})\text{DSS}}$ ,  
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4.
- ⑥ Uses IRLBA1304/P data and test conditions.



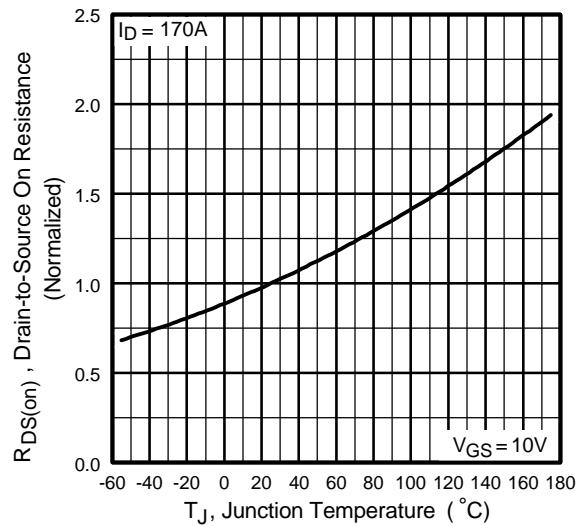
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics



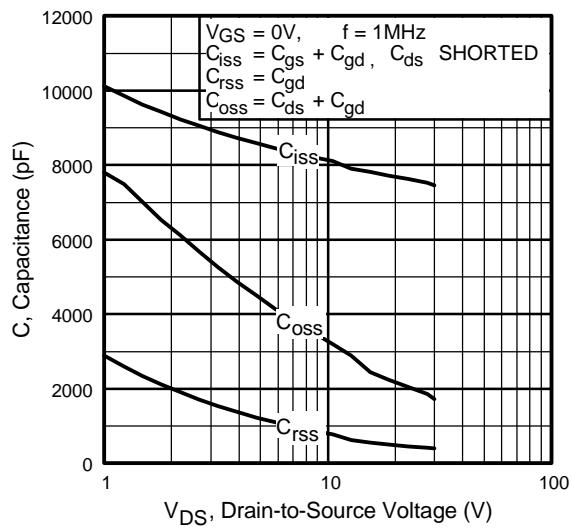
**Fig 3.** Typical Transfer Characteristics



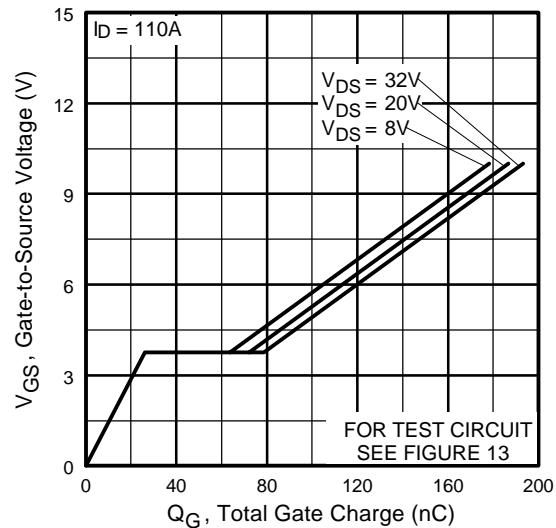
**Fig 4.** Normalized On-Resistance  
Vs. Temperature

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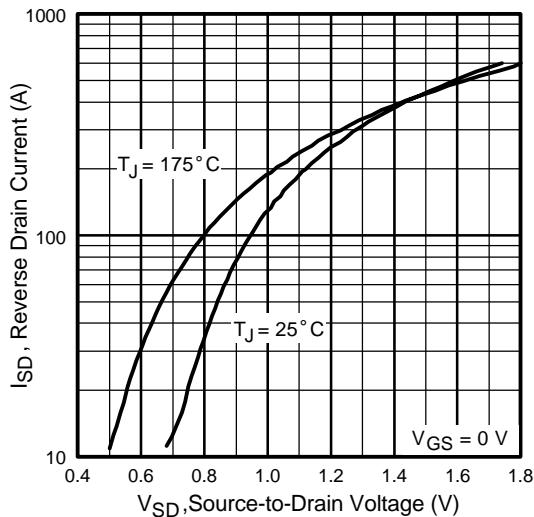
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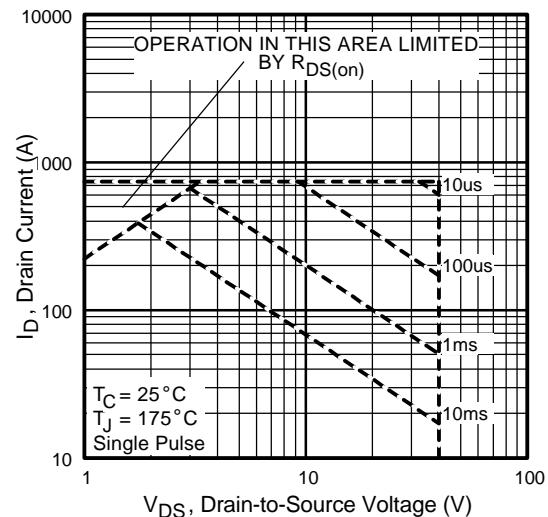
**Fig 5.** Typical Capacitance Vs.  
Drain-to-Source Voltage



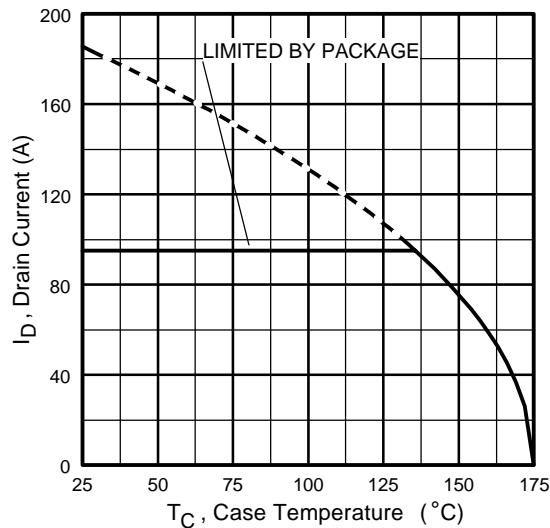
**Fig 6.** Typical Gate Charge Vs.  
Gate-to-Source Voltage



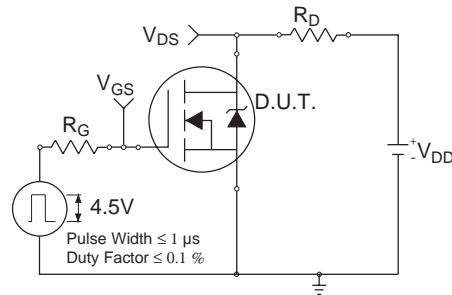
**Fig 7.** Typical Source-Drain Diode  
Forward Voltage



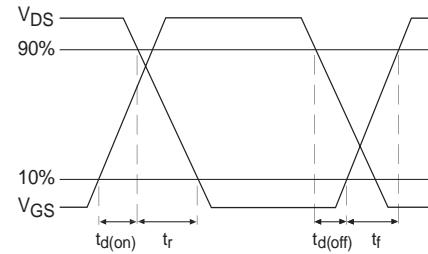
**Fig 8.** Maximum Safe Operating Area



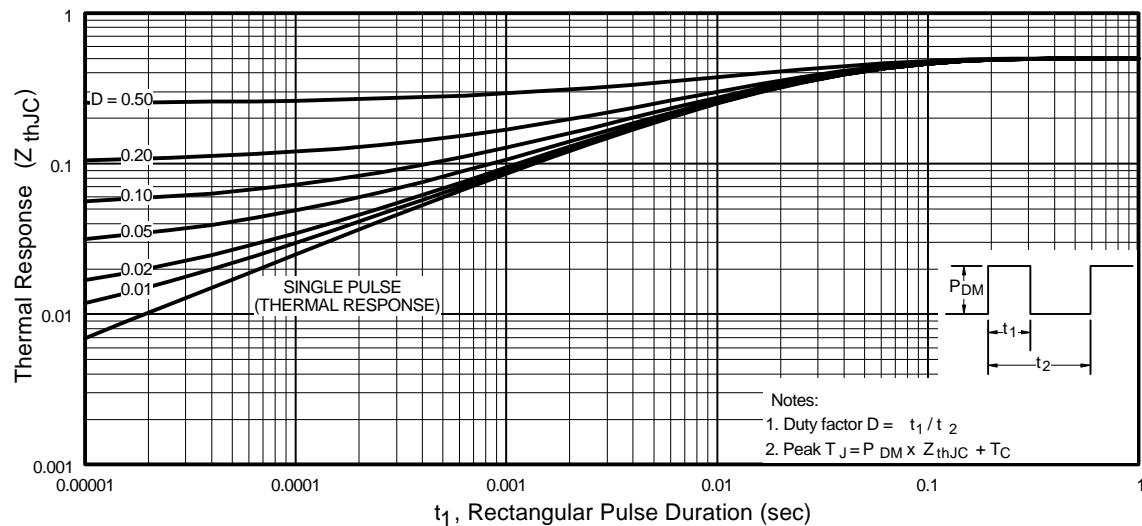
**Fig 9.** Maximum Drain Current Vs.  
Case Temperature



**Fig 10a.** Switching Time Test Circuit



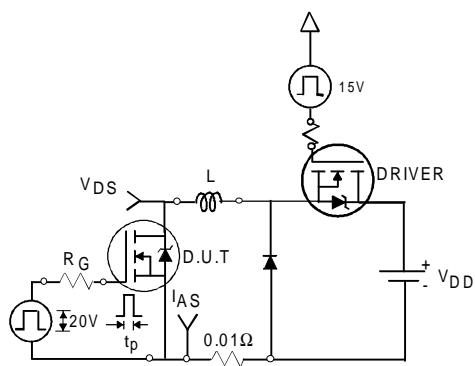
**Fig 10b.** Switching Time Waveforms



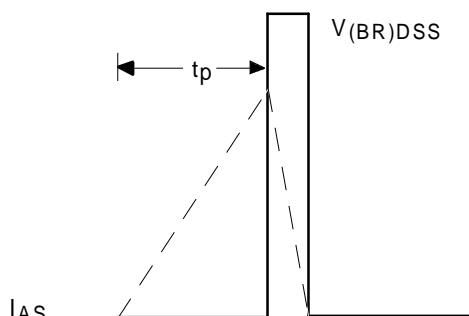
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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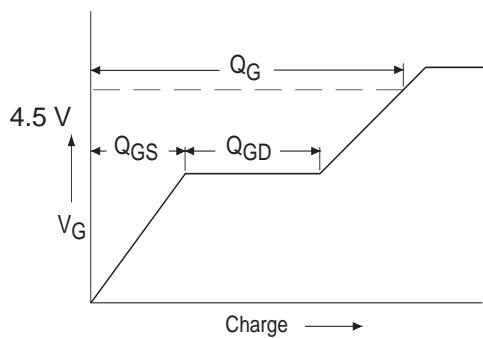
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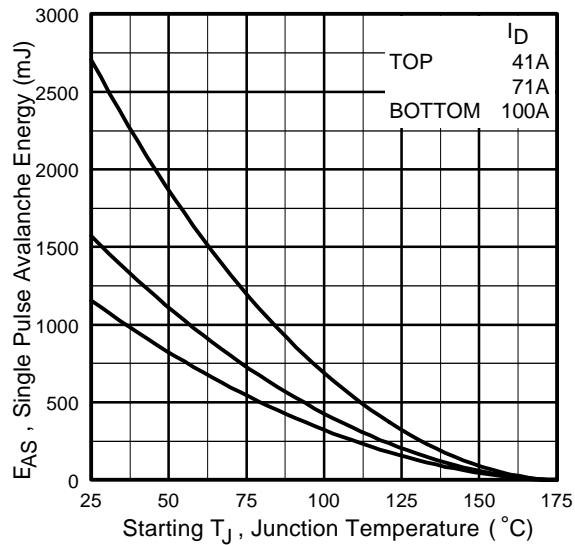
**Fig 12a.** Unclamped Inductive Test Circuit



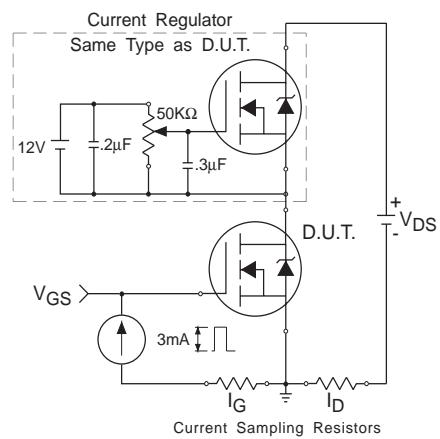
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

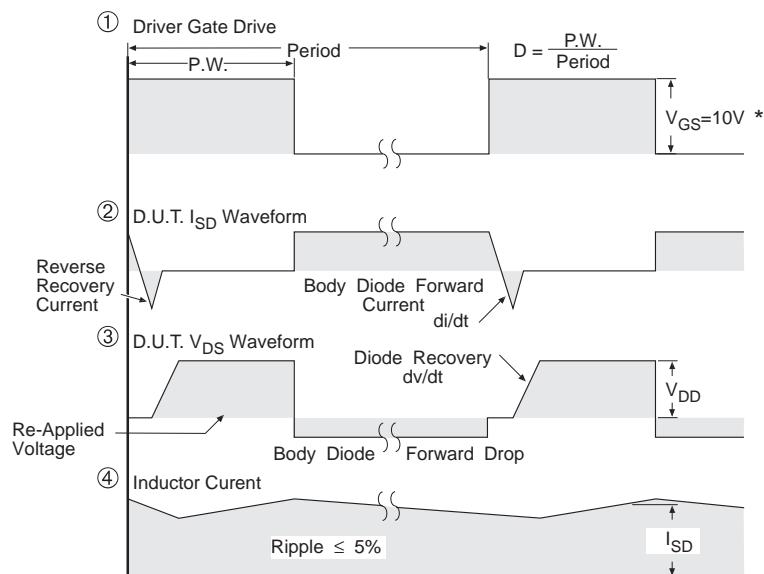
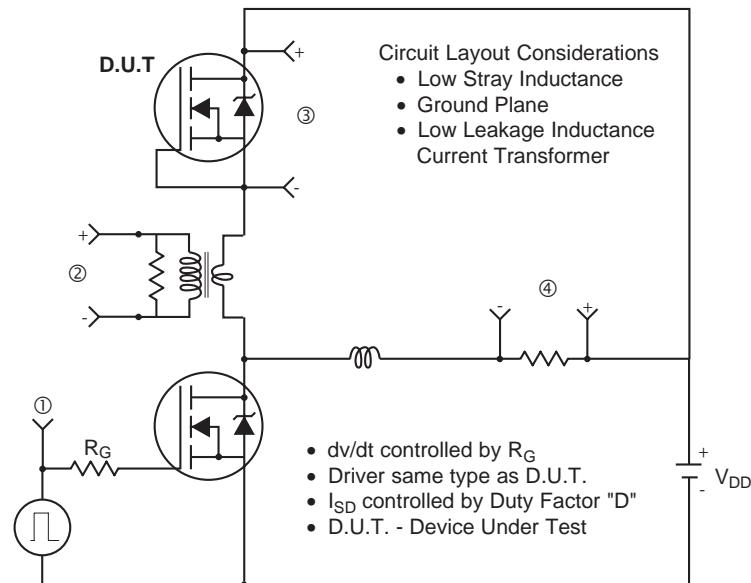


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

### Peak Diode Recovery dv/dt Test Circuit



\*  $V_{GS} = 5V$  for Logic Level Devices

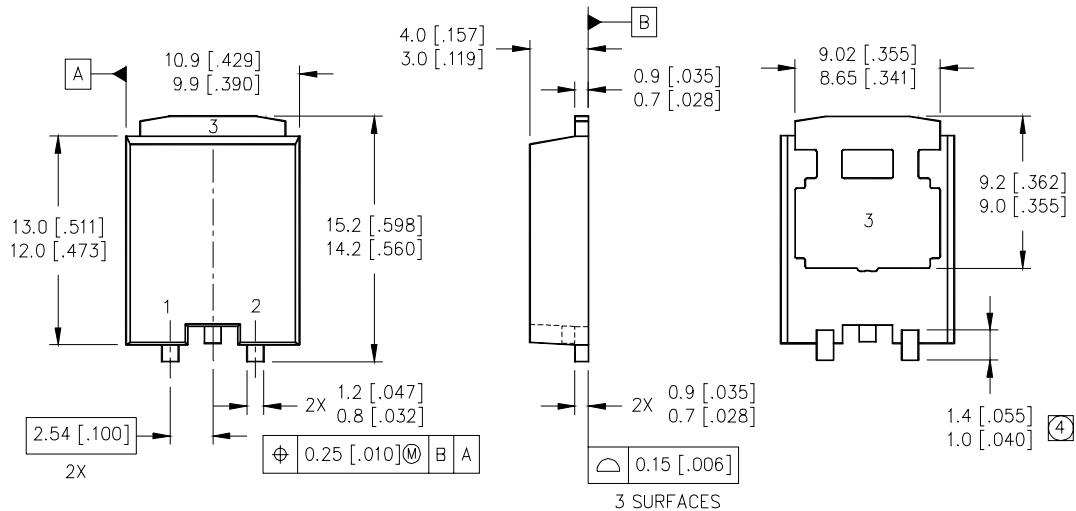
**Fig 14.** For N-Channel HEXFET® Power MOSFETs

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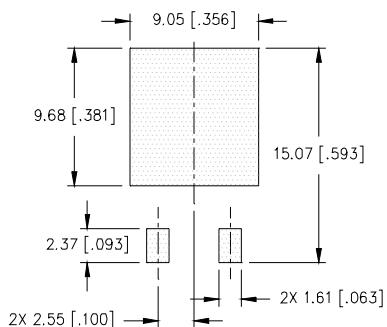
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## Super-D<sup>2</sup>Pak™ Package Outline

Dimensions are shown in millimeters (inches)



### MINIMUM RECOMMENDED FOOTPRINT



### LEAD ASSIGNMENTS

MOSFET	SCHOTTKY / FRED
1 = GATE	1 = ANODE 1
2 = SOURCE	2 = ANODE 2
3 = DRAIN	3 = COMMON CATHODE

### NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- (4) DIMENSION IS MEASURED AT FULL LEAD WIDTH.

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**IR CANADA:** 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200

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*Data and specifications subject to change without notice. 2/00*